54198/74198 8-Bit Parallel-in, Parallel-Out, Bidirectional Shift Register

	Schottky TTL					High-Speed TTL					Low-Power Schottky TTL					Standard TTL					Low-Power TTL				
	Device Type	Package				Device Type	Package				Device Type	Package				Device Type	Package				Device Type	Package			
		C	P	M	CF		C	P	M	CF		C	P	M	CF		C	P	M	CF		C	P	M	CF
T.I.																SN54198	J①			W①					
																SN74198	J①	N①							
FAIRCHILD																FM54198/FM93198	D①								
																FC74198/FC93198	D①								
MOTOROLA																MC54198		①							
																MC74198		①							
N.S.C.																DM54198	J①			F①					
																DM74198	J①	N①		F①					
PHILIPS																									
																N74198		①							
SIGNETICS																S54198	F①	N①		Q①					
																N74198	F①	N①							
SIEMENS																									
																FLJ311		①							
FUJITSU																									
																MB455	①								
HITACHI																									
																HD74198	①	P①							
MITSUBISHI																									
																M53398		P①							
NEC																									
																μPB2198	D①								
TOSHIBA																									

Electrical Characteristics SN54198/SN74198

absolute maximum ratings over operating free-air temperature range

Supply voltage, V_{CC}	7V	Operating free-air temperature range	SN54'	−55°C to	125°C
Input voltage	5.5V		SN74'	0°C to	70°C
		Storage temperature range		−65°C to	150°C

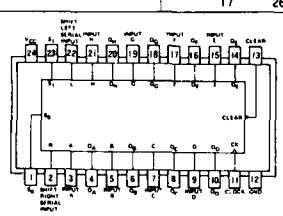
recommended operating conditions

	SN54198			SN74198			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−800			−800	μA
Low-level output current, I_{OL}			16			16	mA
Clock frequency, f_{clock}	0		25	0		25	MHz
Width of clock or clear pulse, t_W	20			20			ns
Mode-control setup time, t_{setup}	30			30			ns
Data setup time, t_{setup}	20			20			ns
Hold time at any input, t_{hold}	0			0			ns
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range

	PARAMETER *	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_I	Input clamp voltage	V_{CC}=MIN, I_I=−12mA				−1.5	V
V_{OH}	High-level output voltage	V_{CC}=MIN, V_{IH}=2V, V_{IL}=0.8V, I_{OH}=−800μA		2.4	3.4		V
V_{OL}	Low-level output voltage	V_{CC}=MIN, V_{IH}=2V, V_{IL}=0.8V, I_{OL}=16mA			0.2	0.4	V
I_I	Input current at maximum input voltage	V_{CC}=MAX, V_I=5.5V				1	mA
I_{IH}	High-level input current	V_{CC}=MAX, V_I=2.4V				40	μA
I_{IL}	Low-level input current	V_{CC}=MAX, V_I=0.4V				−1.6	mA
I_{OS}	Short-circuit output current◆	V_{CC}=MAX	SN54'	−20		−57	mA
			SN74'	−18		−57	
I_{CC}	Supply current	V_{CC}=MAX, See Note 1	SN54'		72	104	mA
			SN74'		72	116	
f_{max}	Maximum input count frequency	V_{CC}=5V, T_A=25°C, C_L=15pF, R_L=400Ω		25	35		MHz
t_{PHL}	from clear				23	35	ns
t_{PHL}	from clock				20	30	ns
t_{PLH}	from clock				17	26	ns

Pin Assignment (Top View)



positive logic : see function table

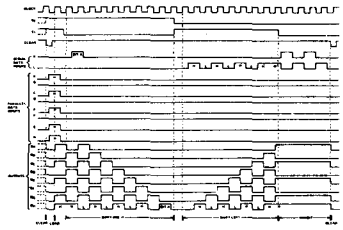
Function Table

198 (See Note2)

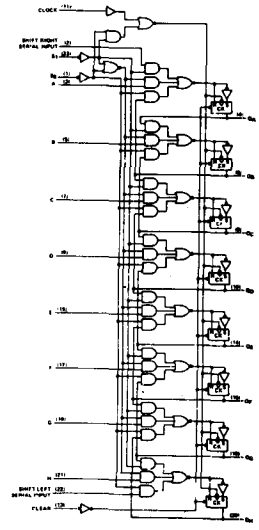
INPUTS							OUTPUTS			
CLEAR	MODE		CLOCK	SERIAL		PARALLEL	Q_A	Q_B ...	Q_G	Q_H
	S_1	S_0		LEFT	RIGHT	A . . . H				
L	X	X	X	X	X	X	L	L	L	L
H	X	X	L	X	X	X	Q_{AO}	Q_{BO}	Q_{GO}	Q_{HO}
H	H	H	↑	X	X	a . . . h	a	b	g	h
H	L	H	↑	X	H	X	H	Q_{An}	Q_{Fn}	Q_{Gn}
H	L	H	↑	X	L	X	L	Q_{An}	Q_{Fn}	Q_{Gn}
H	H	L	↑	H	X	X	Q_{Bn}	Q_{Cn}	Q_{Hn}	H
H	H	L	↑	L	X	X	Q_{Bn}	Q_{Cn}	Q_{Hn}	L
H	L	L	X	X	X	X	Q_{AO}	Q_{BO}	Q_{GO}	Q_{HO}

H=high level (steady state), L=low level (steady state)
X=irrelevant (any input, including transitions) ↑=transition from low to high level

typical clear, load, right-shift, inhibit, and clear sequences



Functional Block Diagram



'198 8-BIT SHIFT GEGISTER

NOTES : 1. With all outputs open, Clear and Inputs A thru H, and 4.5V applied to SO, S1, and the serial inputs, I_{CC} is tested with a momentary GND, then 4.5V, applied to clock.
2. a . . h=the level of stesady-state input at inputs A thru H, respectively.
Q_{AO}, Q_{BO}, Q_{GO}, Q_{HO}=the level of Q_A, Q_B, Q_G, or Q_H, respectively, before the indicated steady-state input conditions were established.
Q_{An}, Q_{Bn}, etc.=the level of Q_A, Q_B, etc., respectively, before the most-recent ↑ transition of the clock.

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡ All typical values are at V_{CC}=5V, T_A=25°C.
◆ Not more than one output should be shorted at a time.
* t_{PLH}=propagation delay time, low-to-high level output
t_{PHL}=propagation delay time, high-to-low-level output