W83194BR-PT

WINBOND

STEPLESS VIA PT MAIN CLOCK GENERATOR

winbond

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1. GENERAL DESCRIPTION

The W83194BR-PT is a Clock Synthesizer for VIA PT chipset. W83194BR-PT provides all clocks required for high-speed microprocessor and provides step-less frequency programming and 32 different frequencies of CPU, PCI, and AGP clocks setting. All clocks are externally selectable with smooth transitions.

The W83194BR-PT provides I^2C serial bus interface to program the registers to enable or disable each clock outputs and provides -0.5% and +/-0.25% center type spread spectrum or programmable S.S.T. scale to reduce EMI.

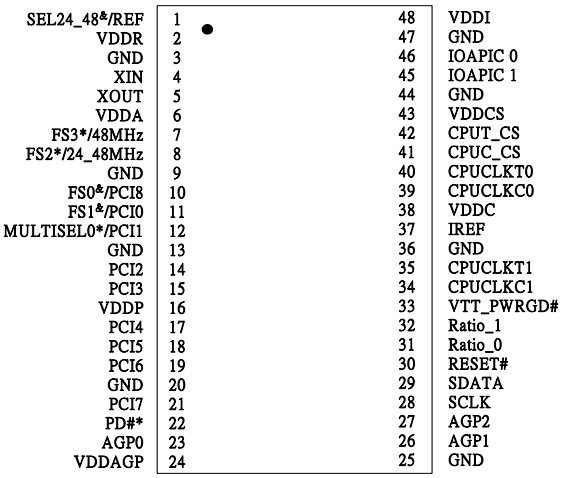
The W83194BR-PT also has watchdog timer and reset output pin to support auto-reset when systems hanging caused by improper frequency setting.

The W83194BR-PT accepts a 14.318 MHz reference crystal as its input and runs on a 3.3V supply.

2. PRODUCT FEATURES

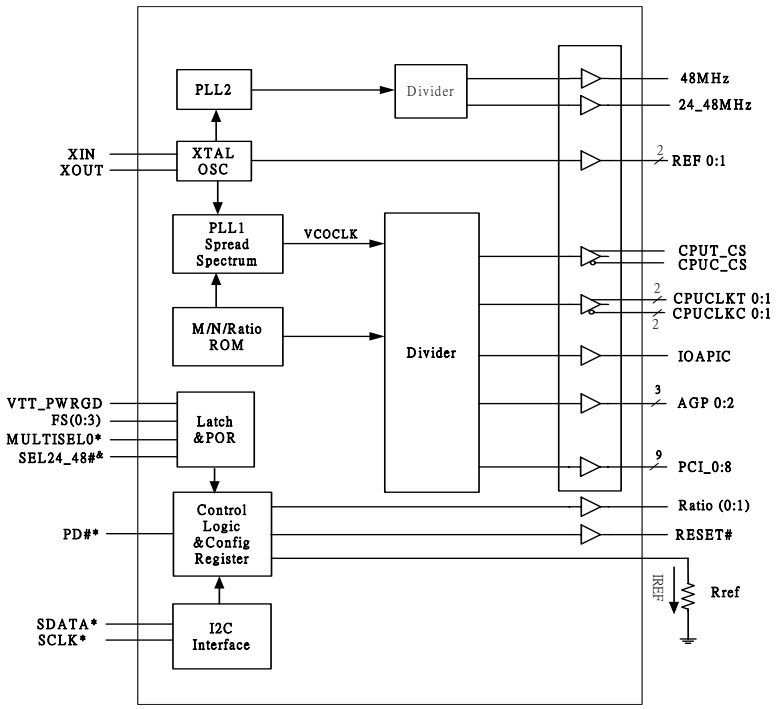
- 2 Differential pairs of CPU clock outputs
- 1 Differential pairs push pull of CPU_CS clock outputs
- 3 AGP clock outputs
- 9 PCI synchronous clocks
- 24_48Mhz clock output for super I/O.
- 48 MHz clock output for USB.
- 2 IOAPIC clock outputs.
- 1 REF clock output.
- Skew form CPU to PCI clock 1 to 4 ns, center 2.6 ns
- Smooth frequency switch with selections from 100 to 200MHz
- Step-less frequency programming
- I^2C 2-Wire serial interface and support byte read/write and block read/write.
- -0.5% and +/- 0.25% center type spread spectrum
- Programmable S.S.T. scale to reduce EMI
- Programmable registers to enable/stop each output and select modes
- Watch Dog Timer and RESET# output pins
- 48-pin SSOP package

3. PIN CONFIGURATION



#: Active low
*: Internal pull up resistor 120K to VDD
&: Internal Pull-down resistor 120K to GND

4. BLOCK DIAGRAM



5. PIN DESCRIPTION

BUFFER TYPE SYMBOL	DESCRIPTION
IN	Input
IN_{tp120k}	Latched input at power up, internal 120kΩ pull up.
IN_{td120k}	Latched input at power up, internal 120kΩ pull down.
OUT	Output
OD	Open Drain
I/O	Bi-directional Pin
I/OD	Bi-directional Pin, Open Drain.
#	Active Low
*	Internal 120kΩ pull-up
&	Internal 120 kΩ pull-down

5.1 Crystal I/O

PIN	PIN NAME	TYPE	DESCRIPTION
4	XIN	IN	Crystal input with internal loading capacitors (18pF) and feedback resistors.
5	XOUT	OUT	Crystal output at 14.318MHz nominally with internal loading capacitors (18pF).

5.2 CPU, AGP, and PCI, IOAPIC Clock Outputs

PIN	PIN NAME	TYPE	DESCRIPTION
34, 35, 39, 40	CPUCLKT [0:1] CPUCLKC [0:1]	OUT	Low skew (< 250ps) differential clock outputs for host frequencies of CPU
41,42	CPUT_CS CPUC_CS	OUT	Low skew (< 250ps) differential push pull clock outputs for host frequencies of CHIPSET
23, 26, 27	AGP0: 2	OUT	3.3V AGP clock outputs.
10	PCI8	OUT	3.3V PCI clock output.
	FS0&	IN_{td120k}	Latched input for FS0 at initial power up for H/W selecting the output frequency. This is internal 120K pull down.
11	PCI0	OUT	3.3V PCI clock output.
	FS1&	IN_{td120k}	Latched input for FS1 at initial power up for H/W selecting the output frequency, This is internal 120K pull down.
12	PCICLK1	OUT	3.3V PCI clock output.
	MULTISEL0*	IN_{tp120k}	Latched input for MULTSEL at initial power up, internal 120K pull up
14, 15, 17, 18, 19, 21	PCI [2:7]	OUT	Low skew (< 250ps) PCI clock outputs.
46, 45	IOAPIC 0:1	OUT	2.5V PCI/2 clock outputs.

5.3 I²C Control Interface

PIN	PIN NAME	TYPE	DESCRIPTION
29	SDATA*	I/OD	Serial data of I2C 2-wire control interface with internal pull-up resistor.
28	SCLK*	IN	Serial clock of I2C 2-wire control interface with internal pull-up resistor.

5.4 Fixed Frequency Outputs

PIN	PIN NAME	TYPE	DESCRIPTION
1	REF	OUT	14.318MHz output.
	SEL24_48&	IN_{td120k}	Latched input for 24MHz or 48MHz select pin. This is internal 120K pull down default 48MHz. In power on reset period, it is a hardware-latched pin, and it can be R/W by I2C control after power on reset period. Select by register 15 bit 7.
7	48MHz	OUT	48MHz clock output for USB.
	FS3*	IN_{tp120k}	Latched input for FS3 at initial power up for H/W selecting the output frequency. This is internal 120K pull up.
8	24_48MHz	OUT	24 or 48MHz (default) clock output, In power on reset period, it is a hardware-latched pin, and it can be R/W by I2C control after power on reset period. Select by register 15 bit 7.
	FS2*	IN_{tp120k}	Latched input for FS2 at initial power up for H/W selecting the output frequency. This is internal 120K pull up.

5.5 Power Management Pins

PIN	PIN NAME	TYPE	DESCRIPTION
33	VTT_PWRGD#	IN	Power good input signal comes from ACPI with LOW active. This 3.3V input is level sensitive strobe used to determine FS [4:0] and MULTISEL input are valid and is ready to sample. This pin is LOW active.
32	Ratio_1	OUT	Gear ratio output to chipset. This output can replace CPU BSEL signal.
31	Ratio_0	OUT	Gear ratio output to chipset. This output can replace CPU BSEL signal.
37	IREF	OUT	Deciding the reference current for the CPUCLK pairs. The pin was connected to the precision resistor tied to ground to decide the appropriate current. There are several modes to select different current via power on trapping the Pin 12 (MULTISEL0). The table is show as follows.
30	RESET#	OD	System reset signal when the watchdog is time out. This pin will generate 250ms low phase when the watchdog timer is timeout.
22	PD#*	IN	Power Down Function. This is power down pin, low active (PD#). Internal 120K pull up

5.6 Power Pins

PIN	PIN NAME	TYPE	DESCRIPTION
2	VDDR	PWR	3.3V power supply for REF.
16	VDDP	PWR	3.3V power supply for PCI.
24	VDDAGP	PWR	3.3V power supply for AGP.
38	VDDC	PWR	3.3V power supply for CPU.
43	VDDCS	PWR	2.5V power supply for CPUCLKT & C _CS.
48	VDDI	PWR	2.5V power supply for IOAPIC.
6	VDDA	PWR	3.3V power for Analog power and 48MHz.
3, 9, 13, 20, 25, 36, 44, 47	GND	PWR	Ground pin

5.7 MULTSEL [1:0] selects Function

MULTSEL1 BYTE 5 BIT 7	MULTSEL0 (PIN 12)	BOARD TARGET TRACE/TERM Z	REFERENCE R, IREF = ADD/(3*RR)	OUTPUT CURRENT	VOH @ Z
0	0	50 Ω	Rr =221 1% IREF = 5.00mA	Ioh=4*IREF	1.0V @ 50
0	0	60 Ω	Rr =221 1% IREF = 5.00mA	Ioh=4*IREF	1.2V @ 60
0	1	50 Ω	Rr =221 1% IREF = 5.00mA	Ioh=5*IREF	1.25V @ 50
0	1	60 Ω	Rr =221 1% IREF = 5.00mA	Ioh=5*IREF	1.5V @ 60
1	0	50 Ω	Rr =221 1% IREF = 5.00mA	Ioh=6*IREF	1.5V @ 50
1	0	60 Ω	Rr =221 1% IREF = 5.00mA	Ioh=6*IREF	1.8V @ 60
1	1	50 Ω	Rr =221 1% IREF = 5.00mA	Ioh=7*IREF	1.75V @ 50
1	1	60 Ω	Rr =221 1% IREF = 5.00mA	Ioh=7*IREF	2.1V @ 50
0	0	50 Ω	Rr =475 1% IREF = 2.32mA	Ioh=4*IREF	0.47V @ 50
0	0	60 Ω	Rr =475 1% IREF = 2.32mA	Ioh=4*IREF	0.56V @ 50
0	1	50 Ω	Rr =475 1% IREF = 2.32mA	Ioh=5*IREF	0.58V @ 50
0	1	60 Ω	Rr =475 1% IREF = 2.32mA	Ioh=5*IREF	0.7V @ 60
1	0	50 Ω	Rr =475 1% IREF = 2.32mA	Ioh=6*IREF	0.7V @ 50
1	0	60 Ω	Rr =475 1% IREF = 2.32mA	Ioh=6*IREF	0.84V @ 60
1	1	50 Ω	Rr =475 1% IREF = 2.32mA	Ioh=7*IREF	0.81V @ 50
1	0	60 Ω	Rr =475 1% IREF = 2.32mA	Ioh=6*IREF	0.97V @ 60

6. FREQUENCY SELECTION BY HARDWARE OR SOFTWARE

This frequency table is used at power on latched FS [4:0] value or software programming at SSEL [4:0] (Register 0 bit 7 ~ 4, 2).

FS4	FS3	FS2	FS1	FS0	CPU (MHZ)	AGP (MHZ)	PCI (MHZ)	IOAPIC (MHZ)	SPREAD %
0	0	0	0	0	101.9	67.9	34.0	17.0	+/-0.25%
0	0	0	0	1	104.9	69.9	35.0	17.5	+/-0.25%
0	0	0	1	0	107.9	72.0	36.0	18.0	+/-0.25%
0	0	0	1	1	111.0	74.0	37.0	18.5	+/-0.25%
0	0	1	0	0	114.0	76.0	38.0	19.0	+/-0.25%
0	0	1	0	1	117.0	78.0	39.0	19.5	+/-0.25%
0	0	1	1	0	120.1	80.0	40.0	20.0	+/-0.25%
0	0	1	1	1	123.1	82.1	41.0	20.5	+/-0.25%
0	1	0	0	0	120.1	72.0	36.0	18.0	+/-0.25%
0	1	0	0	1	123.7	74.2	37.1	18.6	+/-0.25%
0	1	0	1	0	134.0	67.0	33.5	16.8	+/-0.25%
0	1	0	1	1	139.9	69.9	35.0	17.5	+/-0.25%
0	1	1	0	0	143.9	72.0	36.0	18.0	+/-0.25%
0	1	1	0	1	148.0	74.0	37.0	18.5	+/-0.25%
0	1	1	1	0	152.0	76.0	38.0	19.0	+/-0.25%
0	1	1	1	1	156.0	78.0	39.0	19.5	+/-0.25%
1	0	0	0	0	160.1	80.0	40.0	20.0	+/-0.25%
1	0	0	0	1	164.1	82.1	41.0	20.5	+/-0.25%
1	0	0	1	0	166.9	66.7	33.4	16.7	+/-0.25%
1	0	0	1	1	170.2	68.1	34.0	17.0	+/-0.25%
1	0	1	0	0	175.1	70.0	35.0	17.5	+/-0.25%
1	0	1	0	1	120.1	60.0	30.0	15.0	+/-0.25%
1	0	1	1	0	149.8	59.9	30.0	15.0	+/-0.25%
1	0	1	1	1	180.1	60.0	30.0	15.0	+/-0.25%
1	1	0	0	0	100.0	66.6	33.3	16.7	-0.5%
1	1	0	0	1	133.3	66.6	33.3	16.7	-0.5%
1	1	0	1	0	199.9	66.6	33.3	16.7	-0.5%
1	1	0	1	1	166.9	66.7	33.4	16.7	-0.5%
1	1	1	0	0	100.2	66.8	33.4	16.7	+/-0.25%
1	1	1	0	1	133.6	66.8	33.4	16.7	+/-0.25%
1	1	1	1	0	200.5	66.8	33.4	16.7	+/-0.25%
1	1	1	1	1	166.9	66.7	33.4	16.7	+/-0.25%

7. I²C CONTROL AND STATUS REGISTERS

7.1 Register 0: Frequency Select (Default = C4h)

BIT	NAME	PWD	DESCRIPTION
7	SSEL [3]	1	Frequency selection by software via I2C
6	SSEL [2]	1	
5	SSEL [1]	0	
4	SSEL [0]	0	
3	EN_SSEL	0	Enable software program FS [4:0]. 0 = Select frequency by hardware. 1= Select frequency by software I2C - Bit 7~ 4, 2.
2	SSEL [4]	1	Frequency selection bit 4
1	EN_SPSP	0	Enable Spread Spectrum in the frequency table. 0 = Normal 1 = Spread Spectrum enabled
0	EN_SAFE_ FREQ	0	Enable reload safe frequency when the watchdog is timeout. 0 = reload the FS [4:0] latched pins when watchdog time out. 1 = reload the safe frequency bit defined at Register 5 bit 4~0.

7.2 Register 1: CPU Clock Control (1 = Enable, 0 = Stopped) (Default = E3h)

BIT	PIN NO	PWD	DESCRIPTION
7	42, 41	1	CPUT / C_CS output control
6	35, 34	1	CPUCLKT1 / C1 output control
5	40, 39	1	CPUCLKT0 / C0 output control
4	-	0	Reserved. Default: 0 (Read only)
3	-	X	Invert Power on latched value of FS3 pin. Default: 0 (Read only)
2	-	X	Invert Power on latched value of FS2 pin. Default: 0 (Read only)
1	-	X	Invert Power on latched value of FS1 pin. Default: 1 (Read only)
0	-	X	Invert Power on latched value of FS0 pin. Default: 1 (Read only)

7.3 Register 2: PCI Clock Control (1 = Enable, 0 = Stopped) (Default = FFh)

BIT	PIN NO	PWD	DESCRIPTION
7	21	1	PCI7 output control
6	19	1	PCI6 output control
5	18	1	PCI5 output control
4	17	1	PCI4 output control
3	15	1	PCI3 output control
2	14	1	PCI2 output control
1	12	1	PCI1 output control
0	11	1	PCI0 output control

7.4 Register 3: PCI, REF, 48MHz Clock Control (1 = Enable, 0 = Stopped) (Default = F8h)

BIT	PIN NO	PWD	DESCRIPTION
7	7	1	48MHZ output control
6	8	1	24_48MHz output control
5	1	1	REF output control
4	10	1	PCI8 output control
3	-	1	Reserved
2	-	0	Reserved
1	32	X	Invert Ratio_1 read back
0	31	X	Invert Ratio_0 read back

7.5 Register 4:MULTISEL1 IOAPIC, AGP Control (1 = Enable, 0 = Stopped) (Default = 7Fh)

BIT	PIN NO	PWD	DESCRIPTION
7	-	0	MULTISEL1 I2C R/W
6	-	1	Reserved
5	-	1	Reserved
4	45	1	IOAPIC1 output control
3	46	1	IOAPIC0 output control
2	27	1	AGP2 output control
1	26	1	AGP1 output control
0	23	1	AGP0 output control

7.6 Register 5: Watchdog Control (Default = 80h)

BIT	NAME	PWD	DESCRIPTION
7	MULTISEL0	X	Pin 12 MULTISEL0 power on trapping pin data read back (Default = 1)
6	EN_WD	0	Enable Watchdog Timer if set to 1. Set to 0, disable watchdog timer. Read this bit will return a counting state. If timer continues down count, this bit will return 1. Otherwise, this bit will return 0.
5	WD_TIMEOUT	0	Watchdog Timeout Status. If the watchdog is started and timer down counts to zero, this bit will be set to 1. Clear this bit to logic 0, If set to 1, when the watchdog is restart in the next time. This bit is Read Only.
4	SAF_FREQ [4]	0	Watchdog safe frequency bits. These bits will be reloaded into FS [4:0], if the watchdog is timeout and enable reload safe frequency bits.
3	SAF_FREQ [3]	0	
2	SAF_FREQ [2]	0	
1	SAF_FREQ [1]	0	
0	SAF_FREQ [0]	0	

7.7 The Register 6, 7 is reserved for Buffer

7.8 Register 8: Watchdog Timer (Default = 08h)

BIT	NAME	PWD	DESCRIPTION
7	WD_TIME [7]	0	Watchdog timeout time. The bit resolution is 250mS. The default time is 8*250mS = 2.0 seconds. If the watchdog timer is start, this register will be down count. Read this register will return a down count value.
6	WD_TIME [6]	0	
5	WD_TIME [5]	0	
4	WD_TIME [4]	0	
3	WD_TIME [3]	1	
2	WD_TIME [2]	0	
1	WD_TIME [1]	0	
0	WD_TIME [0]	0	

7.9 Register 9: M/N Program (Default = ADh)

BIT	NAME	PWD	DESCRIPTION
7	N_DIV [8]	1	Programmable N divisor value. Bit 7 ~0 are defined in the Register 10.
6	TEST2	0	Test bit 2. Winbond test bit, do not change them.
5	TEST1	1	Test bit 1. Winbond test bit, do not change them.
4	M_DIV [4]	0	Programmable M divisor value.
3	M_DIV [3]	1	
2	M_DIV [2]	1	
1	M_DIV [1]	0	
0	M_DIV [0]	1	

7.10 Register 10: M/N Program (Default = 67h)

BIT	NAME	PWD	DESCRIPTION
7	N_DIV [7]	0	Programmable N divisor value bit 7 ~0. The bit 8 is defined in Register 9.
6	N_DIV [6]	1	
5	N_DIV [5]	1	
4	N_DIV [4]	0	
3	N_DIV [3]	0	
2	N_DIV [2]	1	
1	N_DIV [1]	1	
0	N_DIV [0]	1	

7.11 Register 11: Spread Spectrum Programming (Default = 1Fh)

BIT	NAME	PWD	DESCRIPTION
7	SP_UP [3]	0	Spread Spectrum Up Counter bit 3 ~ bit 0.
6	SP_UP [2]	0	
5	SP_UP [1]	0	
4	SP_UP [0]	1	
3	SP_DOWN [3]	1	Spread Spectrum Down Counter bit 3 ~ bit 0 2's complement representation. Ex: 1 -> 1111; 2 -> 1110; 7 -> 1001; 8 -> 1000
2	SP_DOWN [2]	1	
1	SP_DOWN [1]	1	
0	SP_DOWN [0]	1	

7.12 Register 12: Divisor and Step-less Enable Control (Default = 08h)

BIT	NAME	PWD	DESCRIPTION
7	EN_MN_PROG	0	0: use frequency table 1: use M/N register to program frequency The equation is **VCO freq. = 14.318MHz * (N+4)/ M**. When the watchdog timer is timeout, this will be clear. In this time, the frequency is set to hardware default latched or safe frequency set by EN_SFAE_FREQ (Register 0 bit 0).
6	RATIO_SEL [4]	0	CPU, PCI, AGP, ratio selection. The ratio is shown as following table.
5	RATIO_SEL [3]	0	
4	RATIO_SEL [2]	0	
3	RATIO_SEL [1]	1	
2	RATIO_SEL [0]	0	
1	TEST0	0	Test bit 0. Winbond test bit, do not change them.
0	Reserved	0	

I2C Reg12 Definition

Reg12 Bit6	Reg12 Bit5	Reg12 Bit4	Reg12 Bit3	Reg12 Bit2	CPU	CPU_CS	IOAPIC	AGP	PCI
SSEL4	SSEL3	SSEL2	SSEL1	SSEL0	Ratio	Ratio	Ratio	Ratio	Ratio
0	0	0	0	0	2	2	20	5	10
0	0	0	0	1	2	2	24	6	12
0	0	0	1	0	3	3	24	6	12
0	0	0	1	1	4	4	24	6	12
0	0	1	0	0	3	3	20	5	10
0	0	1	0	1	6	6	24	6	12
0	0	1	1	0	4	4	24	6	12
0	0	1	1	1	4	4	24	6	12
0	1	0	0	0	4	4	24	6	12
0	1	0	0	1	5	5	16	8	16
0	1	0	1	0	5	5	16	8	16
0	1	0	1	1	5	5	24	6	12
0	1	1	0	0	5	5	24	6	12
0	1	1	0	1	5	5	16	8	16
0	1	1	1	0	5	5	20	10	20
0	1	1	1	1	5	5	16	8	16
1	0	0	0	0	5	5	20	10	20
1	0	0	0	1	5	5	20	10	20
1	0	0	1	0	6	6	20	10	20
1	0	0	1	1	6	6	24	6	12
1	0	1	0	0	6	6	16	8	16
1	0	1	0	1	6	6	14	7	14
1	0	1	1	0	6	6	16	8	16
1	0	1	1	1	6	6	14	12	14
1	1	0	0	0	2	2	16	8	16
1	1	0	0	1	3	3	24	12	24
1	1	0	1	0	4	4	16	8	16
1	1	0	1	1	6	6	16	8	16
1	1	1	0	0	2	2	14	7	14
1	1	1	0	1	2	2	24	6	12
1	1	1	1	0	4	4	14	7	14
1	1	1	1	1	4	4	24	6	12

7.13 Register 13: CPU to IOAPIC Skew Control (Default = A7h)

BIT	NAME	PWD	DESCRIPTION
7	CPU_IOAPIC_SKEW [2]	1	CPU to IOAPIC SKEW control
6	Reserved	0	Reserved
5	SPCNT [5]	1	Spread Spectrum Programmable time, the resolution is 280ns
4	SPCNT [4]	0	
3	SPCNT [3]	0	
2	SPCNT [2]	1	
1	SPCNT [1]	1	
0	SPCNT [0]	1	

7.14 Register 14: CPU to PCI and IOAPIC Skew Control (Default = 90h)

BIT	NAME	PWD	DESCRIPTION
7	CPU_PCI_SKEW [2]	1	CPU to PCI skew, Skew resolution is 340ps
6	CPU_PCI_SKEW [1]	0	Expand the skew direction is same as
5	CPU_PCI_SKEW [0]	0	CPU_PCI_SKEW [2:0] setting
4	CPU_AGP_SKEW [2]	1	CPU to AGP Skew, Skew resolution is 340ps
3	CPU_AGP_SKEW [1]	0	Expand the skew direction is same as
2	CPU_AGP_SKEW [0]	0	CPU_AGP_SKEW [2:0] setting
1	CPU_IOAPIC_SKEW [1]	0	CPU to IOAPIC skew control, Skew resolution is 340ps
0	CPU_IOAPIC_SKEW [0]	0	Expand the skew direction is same as CPU_AGP_IOAPIC [2:0] setting

7.15 Register 15: SEL24_48 and CPU to CPUCS skew Control (Default = 04h)

BIT	NAME	PWD	DESCRIPTION
7	SEL24_48	X	In power on reset period, it is a hardware-latched pin, and it can be R/W by I2C control after power on reset period. 1-> 24 MHz, 0->48MHz. Default is 48Mhz
6	Reserved	0	Reserved
5	FIX_AGP_PCI	0	0:normal mode, 1: fix mode
4	SEL [1]	0	AGP & PCI FIX frequency (PCI = AGP/2)
3	SEL [0]	0	SEL [1:0] for AGP 00: 72MHZ 01:64MHZ 10: 77NHZ 11: 67MHZ
2	CPU_CPUCS_SKEW [2]	1	CPU to CPUCS Skew, Skew resolution is 340ps
1	CPU_CPUCS_SKEW [1]	0	Expand the skew direction is same as
0	CPU_CPUCS_SKEW [0]	0	CPU_CPUCS_SKEW [2:0] setting

7.16 Register 16: 24, 48, PCI Slew rate control (Default = FFh)

BIT	NAME	PWD	DESCRIPTION
7	P24SW [1]	1	Pin 8, 24-48MHz clock slew rate control
6	P24SW [0]	1	11: strong, 10: normal, 01:normal, 00:weak
5	P48SW [1]	1	Pin 7, 48MHz clock slew rate control
4	P48SW [0]	1	11: strong, 10: normal, 01:normal, 00:weak
3	PCIASW [1]	1	Pin 11,12,14,15, PCI [0:3] clock slew rate control
2	PCIASW [0]	1	11: strong, 10: normal, 01:normal, 00:weak
1	PCIBSW [1]	1	Pin 17,18,20,21,20, PCI [4:7] clock slew rate control
0	PCIBSW [0]	1	11: strong, 10: normal, 01:normal, 00:weak

7.17 Register 17: PCI, AGP, REF Slew rate control (Default = FCh)

BIT	NAME	PWD	DESCRIPTION
7	PCI8SW [1]	1	Pin 10, PCI8 clock slew rate control
6	PCI8SW [0]	1	11: strong, 10: normal, 01:normal, 00:weak
5	AGPASW [1]	1	Pin 27, AGP2 clock slew rate control
4	AGPASW [0]	1	11: strong, 10: normal, 01:normal, 00:weak
3	AGPBSW [1]	1	Pin 23,26, AGP [0:1] clock slew rate control
2	AGPBSW [0]	1	11: strong, 10: normal, 01:normal, 00:weak
1	REFSW [1]	0	REF clock slew rate control
0	REFSW [0]	0	11: strong, 10: normal, 01:normal, 00:weak

7.18 Register 18: IOAPIC, CPUCS Slew rate control (Default = FFh)

BIT	NAME	PWD	DESCRIPTION
7	IOAPICSW [1]	1	Pin 46,45, IOAPIC [0:1] clock slew rate control
6	IOAPICSW [0]	1	11: strong, 10: normal, 01:normal, 00:weak
5	CPUCSW [1]	1	Pin 41,42 CPUC/T_CS clock slew rate control
4	CPUCSW [0]	1	11: strong, 10: normal, 01:normal, 00:weak
3	Reserved	1	Reserved
2	Reserved	1	
1	Reserved	1	Reserved
0	Reserved	1	

7.19 Register 19: Winbond Chip ID (Read Only) (Default = 81h)

BIT	NAME	PWD	DESCRIPTION
7	CHPI_ID [7]	1	Winbond Chip ID. W83194BR-PT is 0x81.
6	CHPI_ID [6]	0	Winbond Chip ID.
5	CHPI_ID [5]	0	Winbond Chip ID.
4	CHPI_ID [4]	0	Winbond Chip ID.
3	CHPI_ID [3]	0	Winbond Chip ID.
2	CHPI_ID [2]	0	Winbond Chip ID.
1	CHPI_ID [1]	0	Winbond Chip ID.
0	CHPI_ID [0]	1	Winbond Chip ID.

7.20 Register 20: Winbond Chip ID (Read Only) (Default = 7Ch)

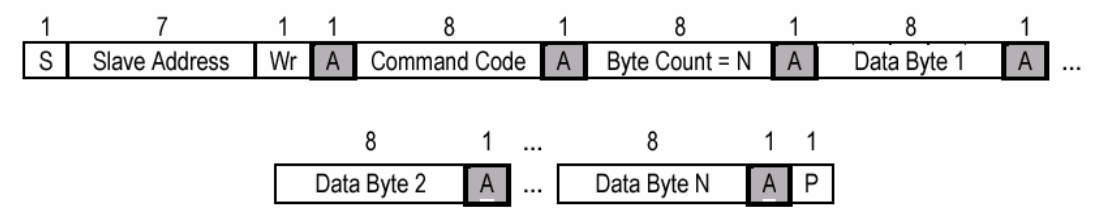
BIT	NAME	PWD	DESCRIPTION
7	MAS_ID [1]	0	MASK definition for master body
6	MAS_ID [0]	1	***A****: 01, ***B****: 10, ***C****: 11, ***D****:00
5	SUB_ID [1]	1	MASK definition for code body
4	SUB_ID [0]	1	*A****001**: 01, *A****002**: 10, *A****003**: 11, *A****004**:00
3	MAS_VER_ID [1]	1	MASK version definition for master body
2	MAS_VER_ID [0]	1	*A****001A**A**: 00, *A****001A**B**: 01, *A****001A**C**: 10, *A****001A**D**: 11.
1	SUB_VER_ID [1]	0	MASK version definition for code body
0	SUB_VER_ID [0]	0	*A****001**A**: 00, *A****001**B**: 01 *A****001**C**: 10, *A****001**D**: 11

8. ACCESS INTERFACE

The W83194BR-PT provides I^{2}C Serial Bus for microprocessor to read/write internal registers. In the W83194BR-PT is provided Block Read/Block Write and Byte-Data Read/Write protocol. The I^{2}C address is defined at 0xD2.

Block Read and Block Write Protocol

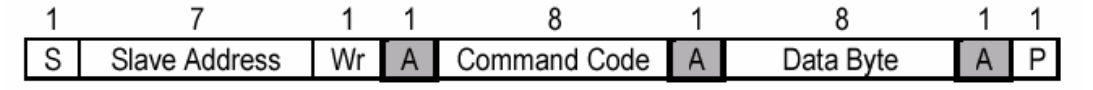
8.1 Block Write protocol



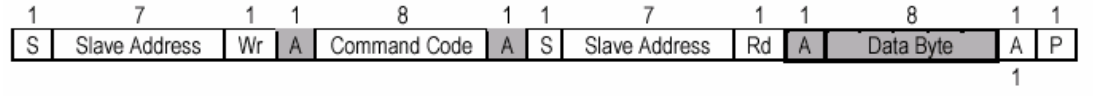
8.2 Block Read protocol

In block mode, the command code must filled 8'h00

8.3 Byte Write protocol



8.4 Byte Read protocol



9. SPECIFICATIONS

9.1 Absolute Maximum Ratings

Stresses greater than those listed in this table may cause permanent damage to the device. Precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. Subjection to maximum conditions for extended periods may affect reliability. Unused inputs must always be tied to an appropriate logic voltage level (Ground or VDD).

PARAMETER	RATING
Absolute 3.3V Core Supply Voltage	-0.5V to +4.6V
Absolute 3.3V I/O Supple Voltage	- 0.5 V to + 4.6 V
Operating 3.3V Core Supply Voltage	3.135V to 3.465V
Operating 3.3V I/O Supple Voltage	3.135V to 3.465V
Storage Temperature	- 65°C to + 150°C
Ambient Temperature	- 55°C to + 125°C
Operating Temperature	0°C to + 70°C
Input ESD Protection (Human body model)	2000V

9.2 General Operating Characteristics

VDDA=VDDAGP=VDDC=VDDR=VDDP= 3.3V ± 5 %, TA = 0℃ to +70℃, Cl=10pF

PARAMETER	SYM.	MIN.	MAX.	UNITS	TEST CONDITIONS
Input Low Voltage	V_{IL}		0.8	V_{dc}	
Input High Voltage	V_{IH}	2.0		V_{dc}	
Output Low Voltage	V_{OL}		0.4	V_{dc}	All outputs using 3.3V power
Output High Voltage	V_{OH}	2.4		V_{dc}	All outputs using 3.3V power
Operating Supply Current	I_{dd}		350	mA	CPU = 100 to 200 MHz PCI = 33.3 Mhz with load
Input pin capacitance	Cin		5	pF	
Output pin capacitance	Cout		6	pF	
Input pin inductance	Lin		7	nH	

9.3 Skew Group Timing Clock

VDDA=VDDAGP=VDDC=VDDR=VDDP= 3.3V ± 5 %, TA = 0℃ to +70℃, Cl=10pF

PARAMETER	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
AGP to PCI Skew	1.5	2.6	3.5	ns	Measured at 1.5V
CPU to CPU Skew			200	ps	Crossing point
AGP to AGP Skew			250	ps	Measured at 1.5V
PCI to PCI Skew			500	ps	Measured at 1.5V
48MHz to 48MHz Skew			1000	ps	Measured at 1.5V
REF to REF Skew			500	ps	Measured at 1.5V

9.4 CPU 0.7V Electrical Characteristics

*VDDA=VDDC= 3.3V ± 5 %, TA = 0℃ to +70℃, Test load Rs=33, Rp=49.9 Cl=10pF, Vr=475, IREF=2.32mA, Ioh=6*IREF*				
PARAMETER	**MIN.**	**MAX.**	**UNITS**	**TEST CONDITIONS**
Rise Time	175	700	ps	100 to 200 Mhz
Fall Time	175	700	ps	100 to 200Mhz
Absolute crossing point Voltages	250	550	mV	100 to 200Mhz
Cycle to Cycle jitter		150	ps	100 to 200Mhz
Duty Cycle	45	55	%	100 to 200Mhz

9.5 CPU 1.0V Electrical Characteristics

*VDDA=VDDC= 3.3V ± 5 %, TA = 0℃ to +70℃, Test load Rs=33, Rp=49.9 Cl=10pF, Vr=221, IREF=5mA, Ioh=4*IREF*				
PARAMETER	**MIN.**	**MAX.**	**UNITS**	**TEST CONDITIONS**
Rise Time	175	700	ps	100 to 200 Mhz
Fall Time	175	700	ps	100 to 200Mhz
Absolute crossing point Voltages	510	760	mV	100 to 200Mhz
Cycle to Cycle jitter		150	ps	100 to 200Mhz
Duty Cycle	45	55	%	100 to 200Mhz

9.6 AGP Electrical Characteristics

VDDAGP= 3.3V ± 5 %, TA = 0℃ to +70℃, Test load, Cl=10pF,				
PARAMETER	**MIN.**	**MAX.**	**UNITS**	**TEST CONDITIONS**
Rise Time	500	2000	ps	Measure from 0.4V to 2.4V
Fall Time	500	2000	ps	Measure from 2.4V to 0.4V
Cycle to Cycle jitter		250	ps	Measure 1.5V point
Duty Cycle	45	55	%	
Pull-Up Current Min	-33		mA	Vout=1.0V
Pull-Up Current Max		-33	mA	Vout=3.135V
Pull-Down Current Min	30		mA	Vout=1.95V
Pull-Down Current Max		38	mA	Vout=0.4V

9.7 PCI Electrical Characteristics

VDDP= 3.3V ± 5 %, TA = 0℃ to +70℃, Test load, Cl=10pF,				
PARAMETER	**MIN.**	**MAX.**	**UNITS**	**TEST CONDITIONS**
Rise Time	500	2000	ps	Measure from 0.4V to 2.4V
Fall Time	500	2000	ps	Measure from 2.4V to 0.4V
Cycle to Cycle jitter		250	ps	Measure 1.5V point
Duty Cycle	45	55	%	
Pull-Up Current Min	-33		mA	Vout=1.0V
Pull-Up Current Max		-33	mA	Vout=3.135V
Pull-Down Current Min	30		mA	Vout=1.95V
Pull-Down Current Max		38	mA	Vout=0.4V

9.8 24M, 48M Electrical Characteristics

VDDA= 3.3V ± 5 %, TA = 0℃ to +70℃, Test load, Cl=10pF,				
PARAMETER	**MIN.**	**MAX.**	**UNITS**	**TEST CONDITIONS**
Rise Time	500	2000	ps	Measure from 0.4V to 2.4V
Fall Time	500	2000	ps	Measure from 2.4V to 0.4V
Long term jitter		500	ps	Measure 1.5V point
Duty Cycle	45	55	%	
Pull-Up Current Min	-33		mA	Vout=1.0V
Pull-Up Current Max		-33	mA	Vout=3.135V
Pull-Down Current Min	30		mA	Vout=1.95V
Pull-Down Current Max		38	mA	Vout=0.4V

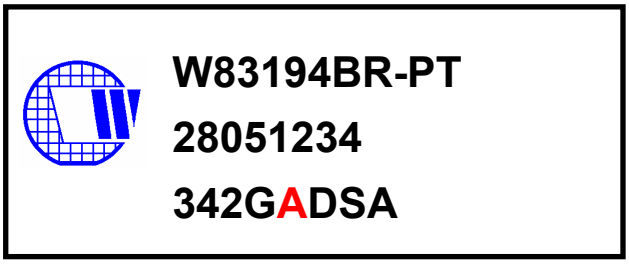
9.9 REF Electrical Characteristics

VDDR= 3.3V ± 5 %, TA = 0℃ to +70℃, Test load, Cl=10pF,				
PARAMETER	**MIN.**	**MAX.**	**UNITS**	**TEST CONDITIONS**
Rise Time	1000	4000	ps	Measure from 0.4V to 2.4V
Fall Time	1000	4000	ps	Measure from 2.4V to 0.4V
Cycle to Cycle jitter		1000	ps	Measure 1.5V point
Duty Cycle	45	55	%	
Pull-Up Current Min	-33		mA	Vout=1.0V
Pull-Up Current Max		-33	mA	Vout=3.135V
Pull-Down Current Min	30		mA	Vout=1.95V
Pull-Down Current Max		38	mA	Vout=0.4V

10. ORDERING INFORMATION

PART NUMBER	PACKAGE TYPE	PRODUCTION FLOW
W83194BR-PT	48 PIN SSOP	Commercial, 0°C to +70°C

11. HOW TO READ THE TOP MARKING



1st line: Winbond logo and the type number: W83194BR-PT

2nd line: Tracking code 2 8051234

2: wafers manufactured in Winbond FAB 2

8051234: wafer production series lot number

3rd line: Tracking code 342 G A D SA

320: packages made in '2003, week 42

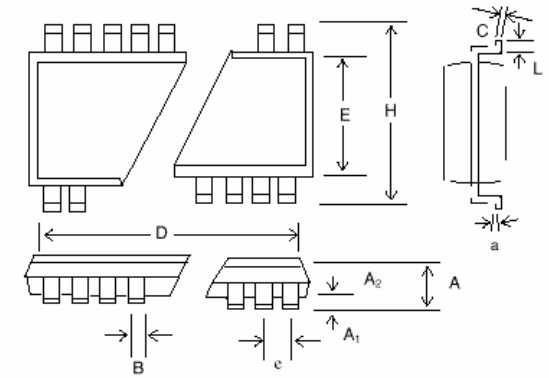
G: assembly house ID; O means OSE, G means GR

A: Internal use code

D: IC revision

SA: mask version

12. PACKAGE DRAWING AND DIMENSIONS



48 PIN SSOP OUTLINE DIMENSIONS

SYMBOL	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	0.110	0	0	2.79
A_1	0.008	0.012	0.016	0.20	0.30	0.41
A2	0.085	0.090	0.095	2.16	2.29	2.41
b	0.008	0.010	0.013	0.20	0.25	0.33
C	0.006	0.008	0.010	0.15	0.20	0.25
D	-	0.625	0.637	-	15.88	16.18
E	0.291	0.295	0.299	7.39	7.49	7.59
e	0.025 BSC			0.64 BSC		
H	0.395	0.408	0.420	10.03	10.36	10.67
L	0.025	0.030	0.040	0.64	0.76	1.02
a	0°	5°	8°	0°	5°	8°

13. REVISION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
			All of the versions before 0.50 are for internal use.
0.5	07/07/03	n.a.	First published preliminary version.
0.6	08/19/03	11, 12	Modify register 14,15 descriptions
0.7	09/30/03	4, 7~13	Modify register 15, add some descriptions
0.8	12/18/03	7, 8, 9, 18	Correction IC version, correction some description and default value
1.0	12/27/04		Update on Web
1.1	4/13/2005	21	Add disclaimer

Important Notice

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