

## TP3054, TP3057

### “Enhanced” Serial Interface CODEC/Filter COMBO® Family

#### General Description

The TP3054, TP3057 family consists of  $\mu$ -law and A-law monolithic PCM CODEC/filters utilizing the A/D and D/A conversion architecture shown in *Figure 1*, and a serial PCM interface. The devices are fabricated using National's advanced double-poly CMOS process (microCMOS).

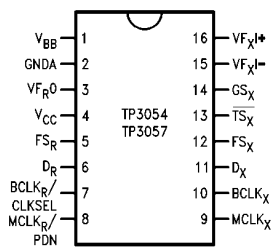
The encode portion of each device consists of an input gain adjust amplifier, an active RC pre-filter which eliminates very high frequency noise prior to entering a switched-capacitor band-pass filter that rejects signals below 200 Hz and above 3400 Hz. Also included are auto-zero circuitry and a companding coder which samples the filtered signal and encodes it in the companded  $\mu$ -law or A-law PCM format. The decode portion of each device consists of an expanding decoder, which reconstructs the analog signal from the companded  $\mu$ -law or A-law code, a low-pass filter which corrects for the  $\sin x/x$  response of the decoder output and rejects signals above 3400 Hz followed by a single-ended power amplifier capable of driving low impedance loads. The devices require two 1.536 MHz, 1.544 MHz or 2.048 MHz transmit and receive master clocks, which may be asynchronous; transmit and receive bit clocks, which may vary from 64 kHz to 2.048 MHz; and transmit and receive frame sync pulses. The timing of the frame sync pulses and PCM data is compatible with both industry standard formats.

#### Features

- Complete CODEC and filtering system (COMBO) including:
  - Transmit high-pass and low-pass filtering
  - Receive low-pass filter with  $\sin x/x$  correction
  - Active RC noise filters
  - $\mu$ -law or A-law compatible Coder and Decoder
  - Internal precision voltage reference
  - Serial I/O interface
  - Internal auto-zero circuitry
- $\mu$ -law, 16-pin—TP3054
- A-law, 16-pin—TP3057
- Designed for D3/D4 and CCITT applications
- $\pm 5V$  operation
- Low operating power—typically 50 mW
- Power-down standby mode—typically 3 mW
- Automatic power-down
- TTL or CMOS compatible digital interfaces
- Maximizes line interface card circuit density
- Dual-In-Line or surface mount packages
- See also AN-370, “Techniques for Designing with CODEC/Filter COMBO Circuits”

#### Connection Diagrams

Dual-In-Line Package



Top View

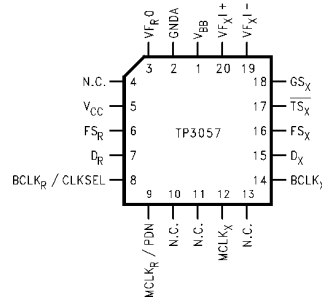
Order Number TP3054J or TP3057J  
See NS Package Number J16A

Order Number TP3054N or TP3057N  
See NS Package Number N16A

Order Number TP3054WM or TP3057WM  
See NS Package Number M16B

TL/H/5510-1

Plastic Chip Carriers



Top View

Order Number TP3057V  
See NS Package Number V20A

TL/H/5510-10

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## Block Diagram

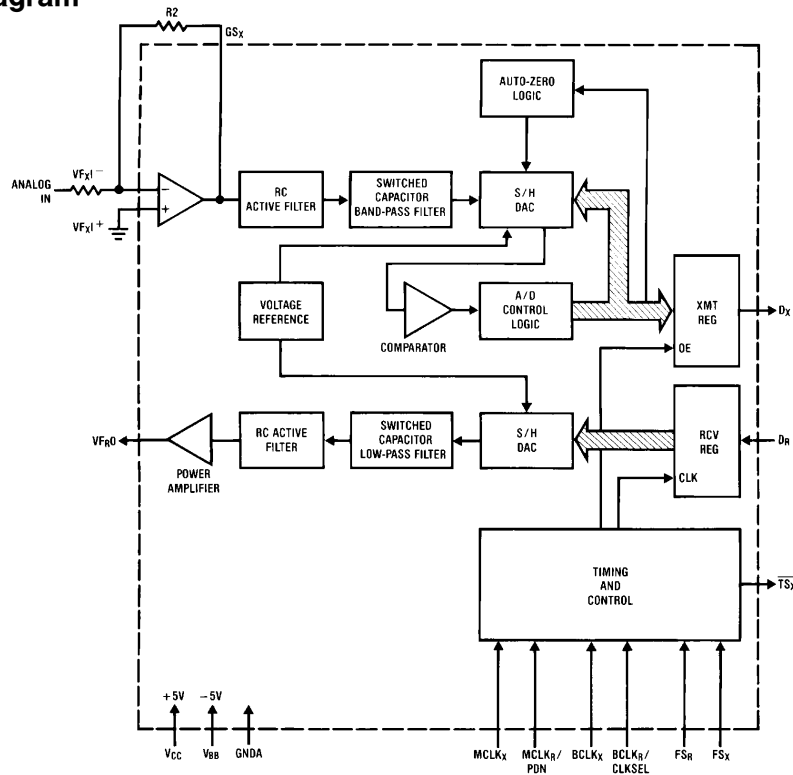


FIGURE 1

TL/H/5510-2

## Pin Description

Symbol	Function	Symbol	Function
$V_{BB}$	Negative power supply pin. $V_{BB} = -5V \pm 5\%$ .	$MCLK_X$	Transmit master clock. Must be 1.536 MHz, 1.544 MHz or 2.048 MHz. May be asynchronous with $MCLK_R$ . Best performance is realized from synchronous operation.
GNDA	Analog ground. All signals are referenced to this pin.	$FS_X$	Transmit frame sync pulse input which enables $BCLK_X$ to shift out the PCM data on $D_X$ . $FS_X$ is an 8 kHz pulse train, see Figures 2 and 3 for timing details.
$VF_{R0}$	Analog output of the receive power amplifier.	$BCLK_X$	The bit clock which shifts out the PCM data on $D_X$ . May vary from 64 kHz to 2.048 MHz, but must be synchronous with $MCLK_X$ .
$V_{CC}$	Positive power supply pin. $V_{CC} = +5V \pm 5\%$ .	$D_X$	The TRI-STATE <sup>®</sup> PCM data output which is enabled by $FS_X$ .
$FS_R$	Receive frame sync pulse which enables $BCLK_R$ to shift PCM data into $D_R$ . $FS_R$ is an 8 kHz pulse train. See Figures 2 and 3 for timing details.	$\overline{TS}_X$	Open drain output which pulses low during the encoder time slot.
$D_R$	Receive data input. PCM data is shifted into $D_R$ following the $FS_R$ leading edge.	$GS_X$	Analog output of the transmit input amplifier. Used to externally set gain.
$BCLK_R/CLKSEL$	The bit clock which shifts data into $D_R$ after the $FS_R$ leading edge. May vary from 64 kHz to 2.048 MHz. Alternatively, may be a logic input which selects either 1.536 MHz/1.544 MHz or 2.048 MHz for master clock in synchronous mode and $BCLK_X$ is used for both transmit and receive directions (see Table I).	$VF_{X1}^-$	Inverting input of the transmit input amplifier.
$MCLK_R/PDN$	Receive master clock. Must be 1.536 MHz, 1.544 MHz or 2.048 MHz. May be asynchronous with $MCLK_X$ , but	$VF_{X1}^+$	Non-inverting input of the transmit input amplifier.

## Functional Description

### POWER-UP

When power is first applied, power-on reset circuitry initializes the COMBO and places it into a power-down state. All non-essential circuits are deactivated and the  $D_X$  and  $V_{FRO}$  outputs are put in high impedance states. To power-up the device, a logical low level or clock must be applied to the  $MCLK_R$ /PDN pin and  $FS_X$  and/or  $FS_R$  pulses must be present. Thus, 2 power-down control modes are available. The first is to pull the  $MCLK_R$ /PDN pin high; the alternative is to hold both  $FS_X$  and  $FS_R$  inputs continuously low—the device will power-down approximately 1 ms after the last  $FS_X$  or  $FS_R$  pulse. Power-up will occur on the first  $FS_X$  or  $FS_R$  pulse. The TRI-STATE PCM data output,  $D_X$ , will remain in the high impedance state until the second  $FS_X$  pulse.

### SYNCHRONOUS OPERATION

For synchronous operation, the same master clock and bit clock should be used for both the transmit and receive directions. In this mode, a clock must be applied to  $MCLK_X$  and the  $MCLK_R$ /PDN pin can be used as a power-down control. A low level on  $MCLK_R$ /PDN powers up the device and a high level powers down the device. In either case,  $MCLK_X$  will be selected as the master clock for both the transmit and receive circuits. A bit clock must also be applied to  $BCLK_X$  and the  $BCLK_R$ /CLKSEL can be used to select the proper internal divider for a master clock of 1.536 MHz, 1.544 MHz or 2.048 MHz. For 1.544 MHz operation, the device automatically compensates for the 193rd clock pulse each frame.

With a fixed level on the  $BCLK_R$ /CLKSEL pin,  $BCLK_X$  will be selected as the bit clock for both the transmit and receive directions. Table 1 indicates the frequencies of operation which can be selected, depending on the state of  $BCLK_R$ /CLKSEL. In this synchronous mode, the bit clock,  $BCLK_X$ , may be from 64 kHz to 2.048 MHz, but must be synchronous with  $MCLK_X$ .

Each  $FS_X$  pulse begins the encoding cycle and the PCM data from the previous encode cycle is shifted out of the enabled  $D_X$  output on the positive edge of  $BCLK_X$ . After 8 bit clock periods, the TRI-STATE  $D_X$  output is returned to a high impedance state. With an  $FS_R$  pulse, PCM data is latched via the  $D_R$  input on the negative edge of  $BCLK_X$  (or  $BCLK_R$  if running).  $FS_X$  and  $FS_R$  must be synchronous with  $MCLK_X/R$ .

TABLE 1. Selection of Master Clock Frequencies

BCLK <sub>R</sub> /CLKSEL	Master Clock Frequency Selected	
	TP3057	TP3054
Clocked	2.048 MHz	1.536 MHz or 1.544 MHz
0	1.536 MHz or 1.544 MHz	2.048 MHz
1	2.048 MHz	1.536 MHz or 1.544 MHz

### ASYNCHRONOUS OPERATION

For asynchronous operation, separate transmit and receive clocks may be applied.  $MCLK_X$  and  $MCLK_R$  must be 2.048 MHz for the TP3057, or 1.536 MHz, 1.544 MHz for the TP3054, and need not be synchronous. For best transmission performance, however,  $MCLK_R$  should be synchronous with  $MCLK_X$ , which is easily achieved by applying only static logic levels to the  $MCLK_R$ /PDN pin. This will automatically connect  $MCLK_X$  to all internal  $MCLK_R$  functions (see Pin Description). For 1.544 MHz operation, the device automatically compensates for the 193rd clock pulse each frame.  $FS_X$  starts each encoding cycle and must be synchronous with  $MCLK_X$  and  $BCLK_X$ .  $FS_R$  starts each decoding cycle and must be synchronous with  $BCLK_R$ .  $BCLK_R$  must be a clock, the logic levels shown in Table 1 are not valid in asynchronous mode.  $BCLK_X$  and  $BCLK_R$  may operate from 64 kHz to 2.048 MHz.

### SHORT FRAME SYNC OPERATION

The COMBO can utilize either a short frame sync pulse or a long frame sync pulse. Upon power initialization, the device assumes a short frame mode. In this mode, both frame sync pulses,  $FS_X$  and  $FS_R$ , must be one bit clock period long, with timing relationships specified in Figure 2. With  $FS_X$  high during a falling edge of  $BCLK_X$ , the next rising edge of  $BCLK_X$  enables the  $D_X$  TRI-STATE output buffer, which will output the sign bit. The following seven rising edges clock out the remaining seven bits, and the next falling edge disables the  $D_X$  output. With  $FS_R$  high during a falling edge of  $BCLK_R$  ( $BCLK_X$  in synchronous mode), the next falling edge of  $BCLK_R$  latches in the sign bit. The following seven falling edges latch in the seven remaining bits. All four devices may utilize the short frame sync pulse in synchronous or asynchronous operating mode.

### LONG FRAME SYNC OPERATION

To use the long frame mode, both the frame sync pulses,  $FS_X$  and  $FS_R$ , must be three or more bit clock periods long, with timing relationships specified in Figure 3. Based on the transmit frame sync,  $FS_X$ , the COMBO will sense whether short or long frame sync pulses are being used. For 64 kHz operation, the frame sync pulse must be kept low for a minimum of 160 ns. The  $D_X$  TRI-STATE output buffer is enabled with the rising edge of  $FS_X$  or the rising edge of  $BCLK_X$ , whichever comes later, and the first bit clocked out is the sign bit. The following seven  $BCLK_X$  rising edges clock out the remaining seven bits. The  $D_X$  output is disabled by the falling  $BCLK_X$  edge following the eighth rising edge, or by  $FS_X$  going low, whichever comes later. A rising edge on the receive frame sync pulse,  $FS_R$ , will cause the PCM data at  $D_R$  to be latched in on the next eight falling edges of  $BCLK_R$  ( $BCLK_X$  in synchronous mode). All four devices may utilize the long frame sync pulse in synchronous or asynchronous mode.

In applications where the LSB bit is used for signalling with  $FS_R$  two bit clock periods long, the decoder will interpret the lost LSB as “1/2” to minimize noise and distortion.

## Functional Description (Continued)

### TRANSMIT SECTION

The transmit section input is an operational amplifier with provision for gain adjustment using two external resistors, see *Figure 4*. The low noise and wide bandwidth allow gains in excess of 20 dB across the audio passband to be realized. The op amp drives a unity-gain filter consisting of RC active pre-filter, followed by an eighth order switched-capacitor bandpass filter clocked at 256 kHz. The output of this filter directly drives the encoder sample-and-hold circuit. The A/D is of companding type according to  $\mu$ -law (TP3054) or A-law (TP3057) coding conventions. A precision voltage reference is trimmed in manufacturing to provide an input overload ( $t_{MAX}$ ) of nominally 2.5V peak (see table of Transmission Characteristics). The  $FS_X$  frame sync pulse controls the sampling of the filter output, and then the successive-approximation encoding cycle begins. The 8-bit code is then loaded into a buffer and shifted out through  $D_X$  at the next  $FS_X$  pulse. The total encoding delay will be approximately 165  $\mu$ s (due to the transmit filter) plus 125  $\mu$ s

(due to encoding delay), which totals 290  $\mu$ s. Any offset voltage due to the filters or comparator is cancelled by sign bit integration.

### RECEIVE SECTION

The receive section consists of an expanding DAC which drives a fifth order switched-capacitor low pass filter clocked at 256 kHz. The decoder is A-law (TP3057) or  $\mu$ -law (TP3054) and the 5th order low pass filter corrects for the  $\sin x/x$  attenuation due to the 8 kHz sample/hold. The filter is then followed by a 2nd order RC active post-filter/power amplifier capable of driving a 600 $\Omega$  load to a level of 7.2 dBm. The receive section is unity-gain. Upon the occurrence of  $FS_R$ , the data at the  $D_R$  input is clocked in on the falling edge of the next eight  $BCLK_R$  ( $BCLK_X$ ) periods. At the end of the decoder time slot, the decoding cycle begins, and 10  $\mu$ s later the decoder DAC output is updated. The total decoder delay is  $\sim 10 \mu$ s (decoder update) plus 110  $\mu$ s (filter delay) plus 62.5  $\mu$ s ( $1/2$  frame), which gives approximately 180  $\mu$ s.

## Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

V <sub>CC</sub> to GNDA	7V
V <sub>BB</sub> to GNDA	-7V
Voltage at any Analog Input or Output	V <sub>CC</sub> + 0.3V to V <sub>BB</sub> - 0.3V

Voltage at any Digital Input or Output	V <sub>CC</sub> + 0.3V to GNDA - 0.3V
Operating Temperature Range	-25°C to +125°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C
ESD (Human Body Model)	2000V
Latch-Up Immunity	= 100 mA on any Pin

**Electrical Characteristics** Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for V<sub>CC</sub> = 5.0V ±5%, V<sub>BB</sub> = -5.0V ±5%; T<sub>A</sub> = 0°C to 70°C by correlation with 100% electrical testing at T<sub>A</sub> = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization. All signals referenced to GNDA. Typical values specified at V<sub>CC</sub> = 5.0V, V<sub>BB</sub> = -5.0V, T<sub>A</sub> = 25°C.

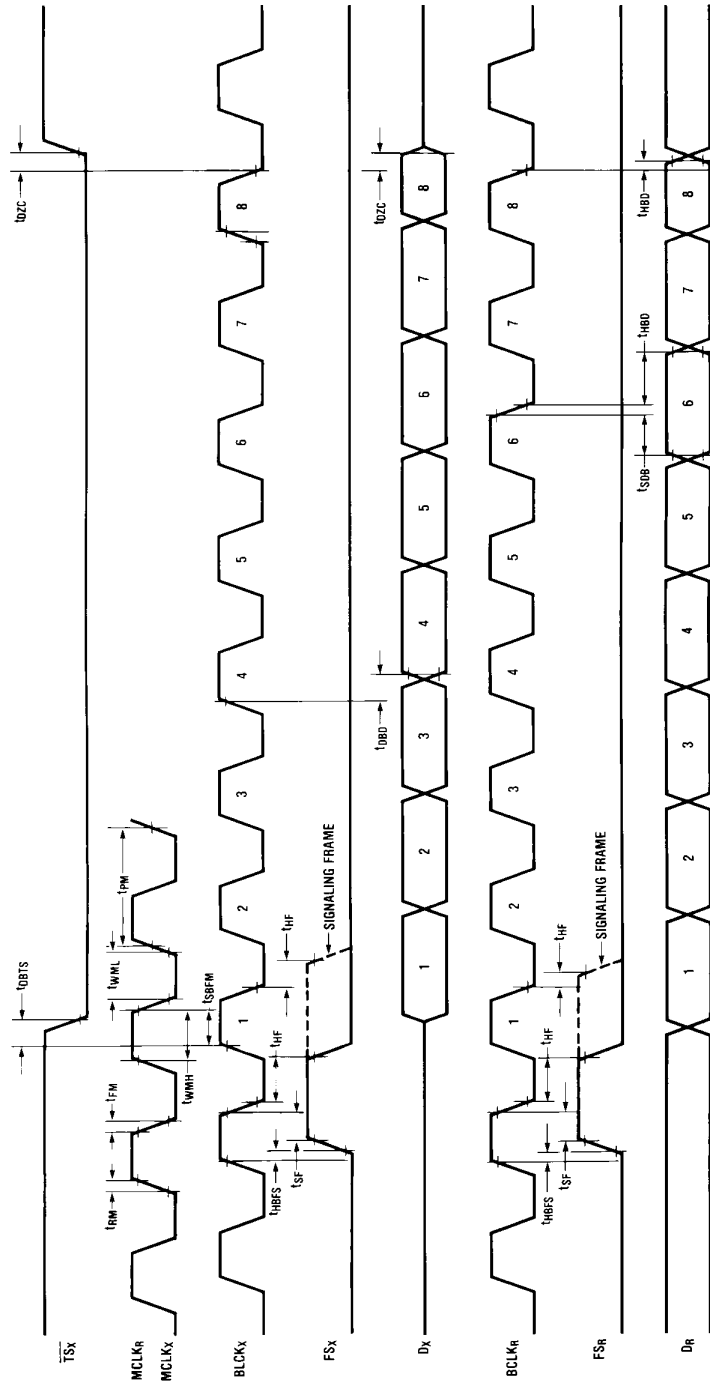
Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>DIGITAL INTERFACE</b>						
V <sub>IL</sub>	Input Low Voltage				<b>0.6</b>	V
V <sub>IH</sub>	Input High Voltage		<b>2.2</b>			V
V <sub>OL</sub>	Output Low Voltage	D <sub>X</sub> , I <sub>L</sub> = 3.2 mA SI <sub>GR</sub> , I <sub>L</sub> = 1.0 mA T <sub>SX</sub> , I <sub>L</sub> = 3.2 mA, Open Drain			<b>0.4</b> <b>0.4</b> <b>0.4</b>	V V V
V <sub>OH</sub>	Output High Voltage	D <sub>X</sub> , I <sub>H</sub> = -3.2 mA SI <sub>GR</sub> , I <sub>H</sub> = -1.0 mA	<b>2.4</b> <b>2.4</b>			V V
I <sub>IL</sub>	Input Low Current	GNDA ≤ V <sub>IN</sub> ≤ V <sub>IL</sub> , All Digital Inputs	-10		<b>10</b>	μA
I <sub>IH</sub>	Input High Current	V <sub>IH</sub> ≤ V <sub>IN</sub> ≤ V <sub>CC</sub>	-10		<b>10</b>	μA
I <sub>OZ</sub>	Output Current in High Impedance State (TRI-STATE)	D <sub>X</sub> , GNDA ≤ V <sub>O</sub> ≤ V <sub>CC</sub>	-10		<b>10</b>	μA
<b>ANALOG INTERFACE WITH TRANSMIT INPUT AMPLIFIER (ALL DEVICES)</b>						
I <sub>XA</sub>	Input Leakage Current	-2.5V ≤ V ≤ +2.5V, VF <sub>XI</sub> <sup>+</sup> or VF <sub>XI</sub> <sup>-</sup>	-200		<b>200</b>	nA
R <sub>IXA</sub>	Input Resistance	-2.5V ≤ V ≤ +2.5V, VF <sub>XI</sub> <sup>+</sup> or VF <sub>XI</sub> <sup>-</sup>	10			MΩ
R <sub>OXA</sub>	Output Resistance	Closed Loop, Unity Gain		1	3	Ω
R <sub>LXA</sub>	Load Resistance	GS <sub>X</sub>	10			kΩ
C <sub>LXA</sub>	Load Capacitance	GS <sub>X</sub>			50	pF
V <sub>OXA</sub>	Output Dynamic Range	GS <sub>X</sub> , R <sub>L</sub> ≥ 10 kΩ	-2.8		<b>2.8</b>	V
A <sub>VXA</sub>	Voltage Gain	VF <sub>XI</sub> <sup>+</sup> to GS <sub>X</sub>	<b>5000</b>			V/V
F <sub>UXA</sub>	Unity Gain Bandwidth		1	2		MHz
V <sub>OSXA</sub>	Offset Voltage		-20		<b>20</b>	mV
V <sub>CMXA</sub>	Common-Mode Voltage	CMRR <sub>XA</sub> > 60 dB	-2.5		2.5	V
CMRR <sub>XA</sub>	Common-Mode Rejection Ratio	DC Test	<b>60</b>			dB
PSRR <sub>XA</sub>	Power Supply Rejection Ratio	DC Test	<b>60</b>			dB
<b>ANALOG INTERFACE WITH RECEIVE FILTER (ALL DEVICES)</b>						
R <sub>ORF</sub>	Output Resistance	Pin VF <sub>RO</sub>		1	3	Ω
R <sub>LRF</sub>	Load Resistance	VF <sub>RO</sub> = ±2.5V	600			Ω
C <sub>LRF</sub>	Load Capacitance				500	pF
V <sub>OSRO</sub>	Output DC Offset Voltage		-200		<b>200</b>	mV
<b>POWER DISSIPATION (ALL DEVICES)</b>						
I <sub>CC0</sub>	Power-Down Current	No Load (Note)		0.5	<b>1.5</b>	mA
I <sub>BB0</sub>	Power-Down Current	No Load (Note)		0.05	<b>0.3</b>	mA
I <sub>CC1</sub>	Power-Up Active Current	No Load		5.0	<b>9.0</b>	mA
I <sub>BB1</sub>	Power-Up Active Current	No Load		5.0	<b>9.0</b>	mA

Note: I<sub>CC0</sub> and I<sub>BB0</sub> are measured after first achieving a power-up state.

**Timing Specifications** Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for  $V_{CC} = 5.0V \pm 5\%$ ,  $V_{BB} = -5.0V \pm 5\%$ ;  $T_A = 0^\circ C$  to  $70^\circ C$  by correlation with 100% electrical testing at  $T_A = 25^\circ C$ . All other limits are assured by correlation with other production tests and/or product design and characterization. All signals referenced to GND. Typical values specified at  $V_{CC} = 5.0V$ ,  $V_{BB} = -5.0V$ ,  $T_A = 25^\circ C$ . All timing parameters are measured at  $V_{OH} = 2.0V$  and  $V_{OL} = 0.7V$ . See Definitions and Timing Conventions section for test methods information.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$1/t_{PM}$	Frequency of Master Clocks	Depends on the Device Used and the BCLK <sub>R</sub> /CLKSEL Pin. MCLK <sub>X</sub> and MCLK <sub>R</sub>		1.536 1.544 <b>2.048</b>		MHz MHz MHz
$t_{RM}$	Rise Time of Master Clock	MCLK <sub>X</sub> and MCLK <sub>R</sub>			50	ns
$t_{FM}$	Fall Time of Master Clock	MCLK <sub>X</sub> and MCLK <sub>R</sub>			50	ns
$t_{PB}$	Period of Bit Clock		485	<b>488</b>	15725	ns
$t_{RB}$	Rise Time of Bit Clock	BCLK <sub>X</sub> and BCLK <sub>R</sub>			50	ns
$t_{FB}$	Fall Time of Bit Clock	BCLK <sub>X</sub> and BCLK <sub>R</sub>			50	ns
$t_{WMH}$	Width of Master Clock High	MCLK <sub>X</sub> and MCLK <sub>R</sub>	<b>160</b>			ns
$t_{WML}$	Width of Master Clock Low	MCLK <sub>X</sub> and MCLK <sub>R</sub>	<b>160</b>			ns
$t_{SBFM}$	Set-Up Time from BCLK <sub>X</sub> High to MCLK <sub>X</sub> Falling Edge	First Bit Clock after the Leading Edge of FS <sub>X</sub>	<b>100</b>			ns
$t_{SFFM}$	Set-Up Time from FS <sub>X</sub> High to MCLK <sub>X</sub> Falling Edge	Long Frame Only	<b>100</b>			ns
$t_{WBH}$	Width of Bit Clock High	$V_{IH} = 2.2V$	<b>160</b>			ns
$t_{WBL}$	Width of Bit Clock Low	$V_{IL} = 0.6V$	<b>160</b>			ns
$t_{HBFL}$	Holding Time from Bit Clock Low to Frame Sync	Long Frame Only	<b>0</b>			ns
$t_{HBFS}$	Holding Time from Bit Clock High to Frame Sync	Short Frame Only	<b>0</b>			ns
$t_{SFB}$	Set-Up Time from Frame Sync to Bit Clock Low	Long Frame Only	<b>80</b>			ns
$t_{DBD}$	Delay Time from BCLK <sub>X</sub> High to Data Valid	Load = 150 pF plus 2 LSTTL Loads	0		140	ns
$t_{DBTS}$	Delay Time to $\overline{TS}_X$ Low	Load = 150 pF plus 2 LSTTL Loads			140	ns
$t_{DZC}$	Delay Time from BCLK <sub>X</sub> Low to Data Output Disabled	$C_L = 0$ pF to 150 pF	50		165	ns
$t_{DZF}$	Delay Time to Valid Data from FS <sub>X</sub> or BCLK <sub>X</sub> , Whichever Comes Later	$C_L = 0$ pF to 150 pF	20		165	ns
$t_{SDB}$	Set-Up Time from D <sub>R</sub> Valid to BCLK <sub>R/X</sub> Low		<b>50</b>			ns
$t_{HBD}$	Hold Time from BCLK <sub>R/X</sub> Low to D <sub>R</sub> Invalid		<b>50</b>			ns
$t_{SF}$	Set-Up Time from FS <sub>X/R</sub> to BCLK <sub>X/R</sub> Low	Short Frame Sync Pulse (1 Bit Clock Period Long)	<b>50</b>			ns
$t_{HF}$	Hold Time from BCLK <sub>X/R</sub> Low to FS <sub>X/R</sub> Low	Short Frame Sync Pulse (1 Bit Clock Period Long)	<b>100</b>			ns
$t_{HBF1}$	Hold Time from 3rd Period of Bit Clock Low to Frame Sync (FS <sub>X</sub> or FS <sub>R</sub> )	Long Frame Sync Pulse (from 3 to 8 Bit Clock Periods Long)	<b>100</b>			ns
$t_{WFL}$	Minimum Width of the Frame Sync Pulse (Low Level)	64k Bit/s Operating Mode	<b>160</b>			ns

# Timing Diagrams



TL/H/5510-3

FIGURE 2. Short Frame Sync Timing





**Transmission Characteristics** Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for  $V_{CC} = 5.0V \pm 5\%$ ,  $V_{BB} = -5.0V \pm 5\%$ ;  $T_A = 0^\circ C$  to  $70^\circ C$  by correlation with 100% electrical testing at  $T_A = 25^\circ C$ . All other limits are assured by correlation with other production tests and/or product design and characterization.  $G_{NDA} = 0V$ ,  $f = 1.02$  kHz,  $V_{IN} = 0$  dBm0, transmit input amplifier connected for unity gain non-inverting. Typical specified at  $V_{CC} = 5.0V$ ,  $V_{BB} = -5.0V$ ,  $T_A = 25^\circ C$ .

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>AMPLITUDE RESPONSE</b>						
	Absolute Levels (Definition of Nominal Gain)	Nominal 0 dBm0 Level is 4 dBm (600Ω) 0 dBm0		1.2276		Vrms
$t_{MAX}$	Virtual Decision Valve Defined Per CCITT Rec. G711	Max Overload Level TP3054 (3.17 dBm0) TP3057 (3.14 dBm0)		2.501 2.492		$V_{PK}$ $V_{PK}$
$G_{XA}$	Transmit Gain, Absolute	$T_A = 25^\circ C$ , $V_{CC} = 5V$ , $V_{BB} = -5V$ Input at $G_{SX} = 0$ dBm0 at 1020 Hz TP3054/57	<b>-0.15</b>		<b>0.15</b>	dB
$G_{XR}$	Transmit Gain, Relative to $G_{XA}$	f = 16 Hz f = 50 Hz f = 60 Hz f = 200 Hz f = 300 Hz – 3000 Hz f = 3300 Hz f = 3400 Hz f = 4000 Hz f = 4600 Hz and Up, Measure Response from 0 Hz to 4000 Hz	<b>-1.8</b> <b>-0.15</b> <b>-0.35</b> <b>-0.7</b>		-40 -30 <b>-26</b> <b>-0.1</b> <b>0.15</b> <b>0.05</b> <b>0</b> <b>-14</b> <b>-32</b>	dB dB dB dB dB dB dB dB dB
$G_{XAT}$	Absolute Transmit Gain Variation with Temperature	Relative to $G_{XA}$	-0.1		0.1	dB
$G_{XAV}$	Absolute Transmit Gain Variation with Supply Voltage	Relative to $G_{XA}$	<b>-0.05</b>		<b>0.05</b>	dB
$G_{XRL}$	Transmit Gain Variations with Level	Sinusoidal Test Method Reference Level = -10 dBm0 $V_{F_{X1}^+} = -40$ dBm0 to +3 dBm0 $V_{F_{X1}^+} = -50$ dBm0 to -40 dBm0 $V_{F_{X1}^+} = -55$ dBm0 to -50 dBm0	<b>-0.2</b> <b>-0.4</b> <b>-1.2</b>		<b>0.2</b> <b>0.4</b> <b>1.2</b>	dB dB dB
$G_{RA}$	Receive Gain, Absolute	$T_A = 25^\circ C$ , $V_{CC} = 5V$ , $V_{BB} = -5V$ Input = Digital Code Sequence for 0 dBm0 Signal at 1020 Hz TP3054/57	<b>-0.15</b>		<b>0.15</b>	dB
$G_{RR}$	Receive Gain, Relative to $G_{RA}$	f = 0 Hz to 3000 Hz f = 3300 Hz f = 3400 Hz f = 4000 Hz	<b>-0.15</b> <b>-0.35</b> <b>-0.7</b>		<b>0.15</b> <b>0.05</b> <b>0</b> <b>-14</b>	dB dB dB dB
$G_{RAT}$	Absolute Receive Gain Variation with Temperature	Relative to $G_{RA}$	-0.1		0.1	dB
$G_{RAV}$	Absolute Receive Gain Variation with Supply Voltage	Relative to $G_{RA}$	<b>-0.05</b>		<b>0.05</b>	dB
$G_{RRL}$	Receive Gain Variations with Level	Sinusoidal Test Method; Reference Input PCM Code Corresponds to an Ideally Encoded PCM Level = -40 dBm0 to +3 dBm0 = -50 dBm0 to -40 dBm0 = -55 dBm0 to -50 dBm0	<b>-0.2</b> <b>-0.4</b> <b>-1.2</b>		<b>0.2</b> <b>0.4</b> <b>1.2</b>	dB dB dB
$V_{RO}$	Receive Output Drive Level	$R_L = 600\Omega$	-2.5		2.5	V

**Transmission Characteristics** (Continued) Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for  $V_{CC} = 5.0V \pm 5\%$ ,  $V_{BB} = -5.0V \pm 5\%$ ;  $T_A = 0^\circ C$  to  $70^\circ C$  by correlation with 100% electrical testing at  $T_A = 25^\circ C$ . All other limits are assured by correlation with other production tests and/or product design and characterization.  $G_{NDA} = 0V$ ,  $f = 1.02$  kHz,  $V_{IN} = 0$  dBm0, transmit input amplifier connected for unity gain non-inverting. Typical values specified at  $V_{CC} = 5.0V$ ,  $V_{BB} = -5.0V$ ,  $T_A = 25^\circ C$ .

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>ENVELOPE DELAY DISTORTION WITH FREQUENCY</b>						
$D_{XA}$	Transmit Delay, Absolute	$f = 1600$ Hz		290	315	$\mu s$
$D_{XR}$	Transmit Delay, Relative to $D_{XA}$	$f = 500$ Hz– $600$ Hz		195	220	$\mu s$
		$f = 600$ Hz– $800$ Hz		120	145	$\mu s$
		$f = 800$ Hz– $1000$ Hz		50	75	$\mu s$
		$f = 1000$ Hz– $1600$ Hz		20	40	$\mu s$
		$f = 1600$ Hz– $2600$ Hz		55	75	$\mu s$
		$f = 2600$ Hz– $2800$ Hz		80	105	$\mu s$
$f = 2800$ Hz– $3000$ Hz		130	155	$\mu s$		
$D_{RA}$	Receive Delay, Absolute	$f = 1600$ Hz		180	200	$\mu s$
$D_{RR}$	Receive Delay, Relative to $D_{RA}$	$f = 500$ Hz– $1000$ Hz	–40	–25		$\mu s$
		$f = 1000$ Hz– $1600$ Hz	–30	–20		$\mu s$
		$f = 1600$ Hz– $2600$ Hz		70	90	$\mu s$
		$f = 2600$ Hz– $2800$ Hz		100	125	$\mu s$
		$f = 2800$ Hz– $3000$ Hz		145	175	$\mu s$
<b>NOISE</b>						
$N_{XC}$	Transmit Noise, C Message Weighted	TP3054		12	<b>15</b>	dBrnC0
$N_{XP}$	Transmit Noise, P Message Weighted	TP3057		–74	<b>–67</b>	dBm0p
$N_{RC}$	Receive Noise, C Message Weighted	PCM Code is Alternating Positive and Negative Zero — TP3054		8	<b>11</b>	dBrnC0
$N_{RP}$	Receive Noise, P Message Weighted	PCM Code Equals Positive Zero — TP3057		–82	<b>–79</b>	dBm0p
$N_{RS}$	Noise, Single Frequency	$f = 0$ kHz to $100$ kHz, Loop Around Measurement, $V_{FXI}^+ = 0$ Vrms			–53	dBm0
$PPSR_X$	Positive Power Supply Rejection, Transmit	$V_{FXI}^+ = -50$ dBm0 $V_{CC} = 5.0 V_{DC} + 100$ mVrms $f = 0$ kHz– $50$ kHz (Note 2)	<b>40</b>			dB
$NPSR_X$	Negative Power Supply Rejection, Transmit	$V_{FXI}^+ = -50$ dBm0 $V_{BB} = -5.0 V_{DC} + 100$ mVrms $f = 0$ kHz– $50$ kHz (Note 2)	<b>40</b>			dB
$PPSR_R$	Positive Power Supply Rejection, Receive	PCM Code Equals Positive Zero $V_{CC} = 5.0 V_{DC} + 100$ mVrms Measure $V_{FR0}$ $f = 0$ Hz– $4000$ Hz	<b>40</b>			dB
		$f = 4$ kHz– $25$ kHz	<b>40</b>			dB
		$f = 25$ kHz– $50$ kHz	<b>36</b>			dB
$NPSR_R$	Negative Power Supply Rejection, Receive	PCM Code Equals Positive Zero $V_{BB} = -5.0 V_{DC} + 100$ mVrms Measure $V_{FR0}$ $f = 0$ Hz– $4000$ Hz	<b>40</b>			dB
		$f = 4$ kHz– $25$ kHz	<b>40</b>			dB
		$f = 25$ kHz– $50$ kHz	<b>36</b>			dB

**Transmission Characteristics** (Continued) Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for  $V_{CC} = 5.0V \pm 5\%$ ,  $V_{BB} = -5.0V \pm 5\%$ ;  $T_A = 0^\circ C$  to  $70^\circ C$  by correlation with 100% electrical testing at  $T_A = 25^\circ C$ . All other limits are assured by correlation with other production tests and/or product design and characterization.  $G_{NDA} = 0V$ ,  $f = 1.02$  kHz,  $V_{IN} = 0$  dBm0, transmit input amplifier connected for unity gain non-inverting. Typical specified at  $V_{CC} = 5.0V$ ,  $V_{BB} = -5.0V$ ,  $T_A = 25^\circ C$ .

Symbol	Parameter	Conditions	Min	Typ	Max	Units
SOS	Spurious Out-of-Band Signals at the Channel Output	Loop Around Measurement, 0 dBm0, 300 Hz to 3400 Hz Input PCM Code Applied at $D_R$ .			-30	dB
		4600 Hz-7600 Hz			-30	dB
		7600 Hz-8400 Hz			-40	dB
		8400 Hz-100,000 Hz			-30	dB

**DISTORTION**

STD <sub>X</sub> STD <sub>R</sub>	Signal to Total Distortion Transmit or Receive Half-Channel	Sinusoidal Test Method (Note 3) Level = 3.0 dBm0 = 0 dBm0 to -30 dBm0 = -40 dBm0 XMT RCV = -55 dBm0 XMT RCV	<b>33</b> <b>36</b> <b>29</b> <b>30</b> <b>14</b> <b>15</b>			dBC dBC dBC dBC dBC dBC
SFD <sub>X</sub>	Single Frequency Distortion, Transmit				<b>-46</b>	dB
SFD <sub>R</sub>	Single Frequency Distortion, Receive				<b>-46</b>	dB
IMD	Intermodulation Distortion	Loop Around Measurement, $V_{F_X^+} = -4$ dBm0 to $-21$ dBm0, Two Frequencies in the Range 300 Hz-3400 Hz			<b>-41</b>	dB

**CROSSTALK**

CT <sub>X-R</sub>	Transmit to Receive Crosstalk, 0 dBm0 Transmit Level	$f = 300$ Hz-3400 Hz $D_R =$ Quiet PCM Code			-90	<b>-75</b>	dB
CT <sub>R-X</sub>	Receive to Transmit Crosstalk, 0 dBm0 Receive Level	$f = 300$ Hz-3400 Hz, $V_{F_X^+} =$ Multitone (Note 2)			-90	<b>-70</b>	dB

**ENCODING FORMAT AT  $D_X$  OUTPUT**

	TP3054 $\mu$ -Law	TP3057 A-Law (Includes Even Bit Inversion)
$V_{IN}$ (at $GS_X$ ) = + Full-Scale	1 0 0 0 0 0 0 0 0	1 0 1 0 1 0 1 0
$V_{IN}$ (at $GS_X$ ) = 0V	$\begin{cases} 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 \\ 0 & 1 & 1 & 1 & 1 & 1 & 1 & 1 \end{cases}$	$\begin{cases} 1 & 1 & 0 & 1 & 0 & 1 & 0 & 1 \\ 0 & 1 & 0 & 1 & 0 & 1 & 0 & 1 \end{cases}$
$V_{IN}$ (at $GS_X$ ) = - Full-Scale	0 0 0 0 0 0 0 0	0 0 1 0 1 0 1 0

**Note 1:** Measured by extrapolation from the distortion test result at -50 dBm0.

**Note 2:** PPSR<sub>X</sub>, NPSR<sub>X</sub>, and CT<sub>R-X</sub> are measured with a -50 dBm0 activation signal applied to  $V_{F_X^+}$ .

**Note 3:** Devices are measured using C message weighted filter for  $\mu$ -Law and psophometric weighted filter for A-Law.

## Applications Information

### POWER SUPPLIES

While the pins of the TP305X family are well protected against electrical misuse, it is recommended that the standard CMOS practice be followed, ensuring that ground is connected to the device before any other connections are made. In applications where the printed circuit board may be plugged into a "hot" socket with power and clocks already present, an extra long ground pin in the connector should be used.

All ground connections to each device should meet at a common point as close as possible to the GNDA pin. This minimizes the interaction of ground return currents flowing through a common bus impedance. 0.1  $\mu$ F supply decoupling capacitors should be connected from this common ground point to  $V_{CC}$  and  $V_{BB}$ , as close to the device as possible.

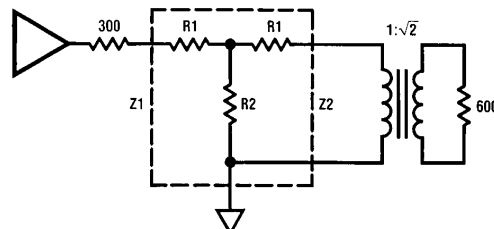
For best performance, the ground point of each CODEC/FILTER on a card should be connected to a common card ground in star formation, rather than via a ground bus.

This common ground point should be decoupled to  $V_{CC}$  and  $V_{BB}$  with 10  $\mu$ F capacitors.

### RECEIVE GAIN ADJUSTMENT

For applications where a TP305X family CODEC/filter receive output must drive a 600 $\Omega$  load, but a peak swing lower than  $\pm 2.5V$  is required, the receive gain can be easily adjusted by inserting a matched T-pad or  $\pi$ -pad at the output. Table II lists the required resistor values for 600 $\Omega$  terminations. As these are generally non-standard values, the equations can be used to compute the attenuation of the closest practical set of resistors. It may be necessary to use unequal values for the R1 or R4 arms of the attenuators to achieve a precise attenuation. Generally it is tolerable to allow a small deviation of the input impedance from nominal while still maintaining a good return loss. For example a 30 dB return loss against 600 $\Omega$  is obtained if the output impedance of the attenuator is in the range 282 $\Omega$  to 319 $\Omega$  (assuming a perfect transformer).

T-Pad Attenuator



$$R1 = Z1 \left( \frac{N^2 + 1}{N^2 - 1} \right) - 2\sqrt{Z1 \cdot Z2} \left( \frac{N}{N^2 - 1} \right)$$

$$R2 = 2\sqrt{Z1 \cdot Z2} \left( \frac{N}{N^2 - 1} \right)$$

$$\text{Where: } N = \sqrt{\frac{\text{POWER IN}}{\text{POWER OUT}}}$$

and

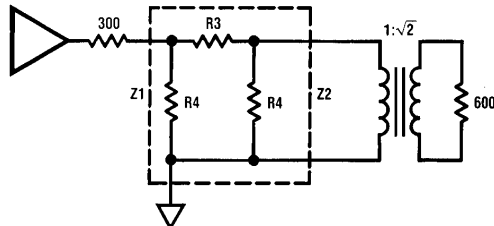
$$S = \sqrt{\frac{Z1}{Z2}}$$

$$\text{Also: } Z = \sqrt{Z_{SC} \cdot Z_{OC}}$$

Where  $Z_{SC}$  = impedance with short circuit termination

and  $Z_{OC}$  = impedance with open circuit termination

$\pi$ -Pad Attenuator



$$R3 = \sqrt{\frac{Z1 \cdot Z2}{2}} \left( \frac{N^2 - 1}{N} \right)$$

$$R3 = Z1 \left( \frac{N^2 - 1}{N^2 - 2NS + 1} \right)$$

TL/H/5510-5

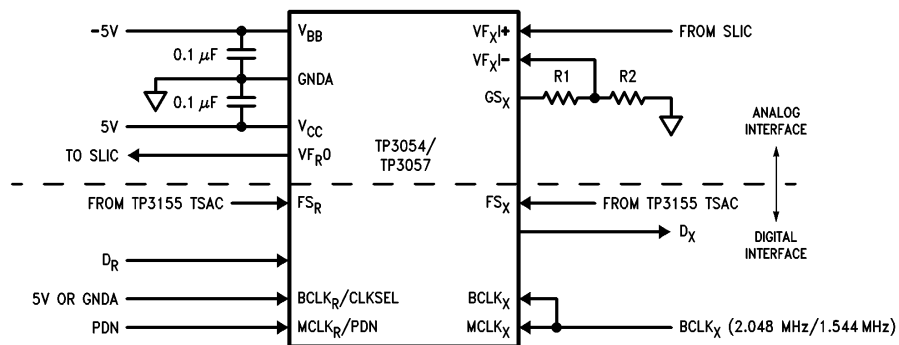
Note: See Application Note 370 for further details.

## Applications Information (Continued)

**TABLE II. Attenuator Tables for Z1 = Z2 = 300Ω**  
(All Values in Ω)

dB	R1	R2	R3	R4
0.1	1.7	26k	3.5	52k
0.2	3.5	13k	6.9	26k
0.3	5.2	8.7k	10.4	17.4k
0.4	6.9	6.5k	13.8	13k
0.5	8.5	5.2k	17.3	10.5k
0.6	10.4	4.4k	21.3	8.7k
0.7	12.1	3.7k	24.2	7.5k
0.8	13.8	3.3k	27.7	6.5k
0.9	15.5	2.9k	31.1	5.8k
1.0	17.3	2.6l	34.6	5.2k
2	34.4	1.3k	70	2.6k
3	51.3	850	107	1.8k
4	68	650	144	1.3k
5	84	494	183	1.1k
6	100	402	224	900
7	115	380	269	785
8	379	284	317	698
9	143	244	370	630
10	156	211	427	527
11	168	184	490	535
12	180	161	550	500
13	190	142	635	473
14	200	125	720	450
15	210	110	816	430
16	218	98	924	413
18	233	77	1.17k	386
20	246	61	1.5k	366

## Typical Synchronous Application

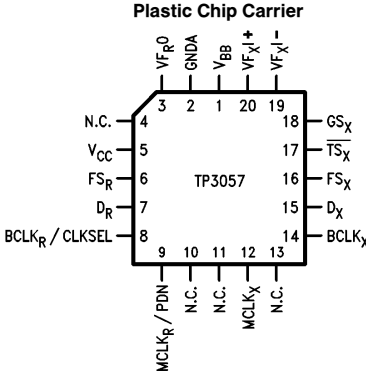


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Note 1: XMIT gain =  $20 \times \log \left( \frac{R1 + R2}{R2} \right)$  where  $(R1 + R2) > 10 \text{ K}\Omega$ .

**FIGURE 4**

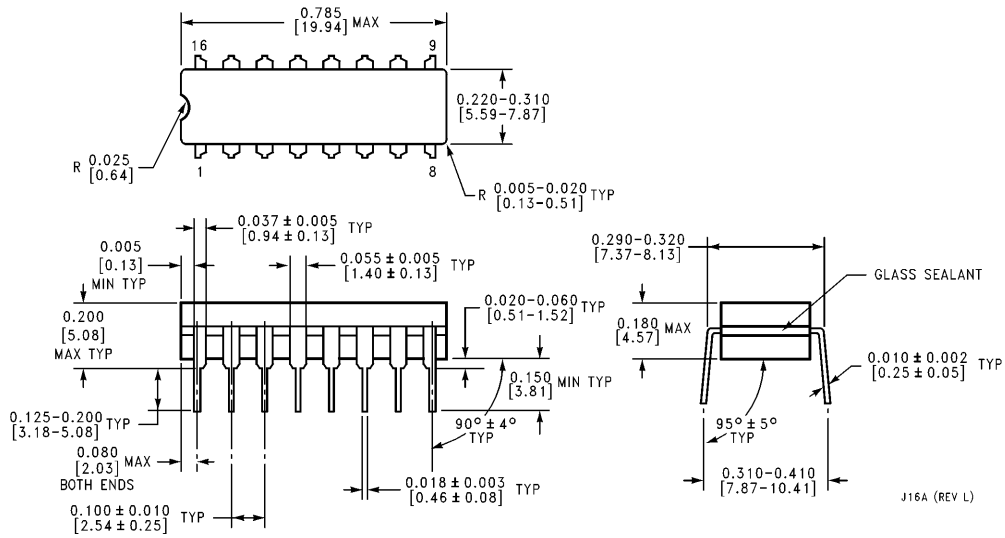
**Connection Diagrams** (Continued)



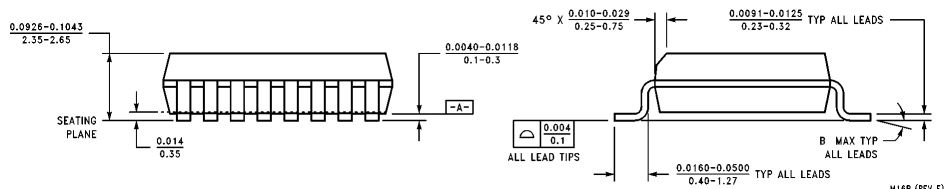
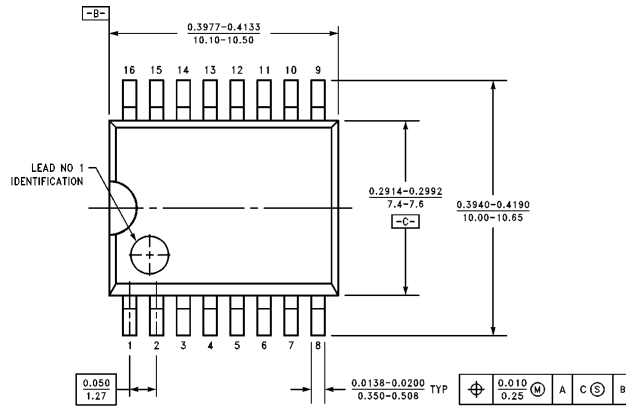
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**Top View**  
**Order Number TP3057V**  
**See NS Package Number V20A**

**Physical Dimensions** inches (millimeters)

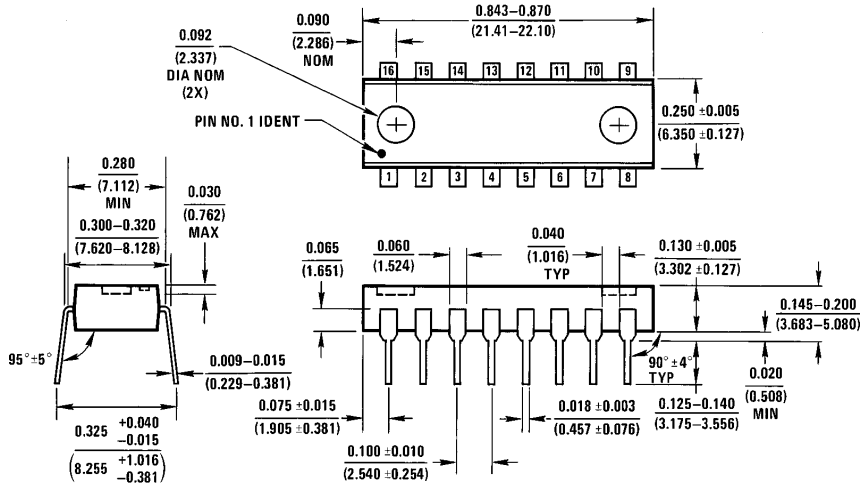


**Cavity Dual-In-Line Package (J)**  
**Order Number TP3054J or TP3057J**  
**NS Package Number J16A**



**Molded Small Outline Package (WM)**  
**Order Number TP3054WM or TP3057WM**  
**NS Package Number M16B**

**Physical Dimensions** inches (millimeters) (Continued)



**Molded Dual-In-Line Package (N)**  
**Order Number TP3054N or TP3057N**  
**NS Package Number N16A**

N16A (REV E)

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