54H71/74H71 AND-OR-Gated J-K Master-Slave Flip-Flop with Preset
54L71/74L71 AND-Gated R-S Master-Slave Flip-Flop with Preset and clear

	Schottky TTL					High-Speed TTL					Low-Power Schottky TTL					Standard TTL					Low-Power TTL				
	Device Type	Package				Device Type	Package				Device Type	Package				Device Type	Package				Device Type	Package			
		C	P	M	CF		C	P	M	CF		C	P	M	CF		C	P	M	CF		C	P	M	CF
T.I.						SN54H71	J①			W②											SN54L71	J③	N③		T④
						SN74H71	J①	N①													SN74L71	J③	N③		T④
FAIRCHILD						FM54H71/FM9H71	D①			F②															
						FC74H71/FC9H71	D①	P①		F②															
MOTOROLA						MC3154	L①			F①															
						MC3054	L①	P①		F①															
N.S.C.						DM54H71	J①	N①													DM54L71	J③	N③		F④
						DM74H71	J①	N①													DM74L71	J③	N③		F④
PHILIPS						N74H71			①																
SIGNETICS						S54H71	F①	A①		W②															
						N74H71	F①	A①																	
SIEMENS																									
FUJITSU																									
HITACHI																									
MITSUBISHI																									
NEC																									
TOSHIBA																									

Electrical Characteristics SN54H71/SN74H71

absolute maximum ratings over operating free-air temperature range

Supply voltage V_{CC}		7V	Operating free-air	SN54H'	−55°C to 125°C
Input voltage		5.5V	temperature range	SN74H'	0°C to 70°C
			Storage temperature range		−65°C to 150°C

recommend operating conditions

			SN54H71			SN74H71			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage V_{CC}			4.5	5	5.5	4.75	5	5.25	V
High-level output current I_{HO}					−500			−500	μA
Low-level output I_{OL}					20			20	mA
Pulse width t_w	Clock high		12			12			ns
	Clock low		28			28			
	Clear or preset L_{OW}		16			16			
Setup time t_{setup}	High-level data		0↑§			0↑§			ns
	Low-level data		0↑§			0↑§			
Hold time t_{hold}			0↓§			0↓§			ns
Operating free-air temperature T_A			−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range

PARAMETER *		TEST CONDITIONS †	MIN	TYP ‡	MAX	UNIT
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
V_I	Input clamp voltage	$V_{CC}=MIN$, $I_I=-8\,mA$			−1.5	V
V_{OH}	High-level output voltage	$V_{CC}=MIN$, $V_{IH}=2V$, $V_{IL}=0.8V$, $I_{OH}=MAX$	2.4	3.4		V
V_{OL}	Low-level output voltage	$V_{CC}=MIN$, $V_{IH}=2V$, $V_{IL}=0.8V$, $I_{OL}=20mA$		0.2	0.4	V
I_I	Input current at maximum input voltage	$V_{CC}=MAX$, $V_I=5.5V$			1	mA
I_{IH}	High-level input current	D, J, or K	$V_{CC}=MAX$, $V_I=2.4V$			50	μA
		Preset				150	
		Clock				100	
I_{IL}	Low-level input current	D, J, or K	$V_{CC}=MAX$, $V_I=0.4V$			−2	mA
		Preset				−6	
		Clock				−4	
I_{OS}	Short-circuit output current ◆	$V_{CC}=MAX$	−40		−100	mA
I_{CC}	Supply current (Average per flip-flop)	$V_{CC}=MAX$, See Note 1	Series 54H		19	30	mA
			Series 74H		19	30	
f_{max}	maximum clock frequency		25	30		MHz
t_{PLH}	from Preset to output Q (as applicable)			6	13	ns
t_{PHL}	from Preset to output $\bar{Q}$ (as applicable)	$V_{CC}=5V$, $T_A=25°C$, $C_L=25pF$, $R_L=280\Omega$		12	24	
t_{PLH}	from Clear to output $\bar{Q}$ (as applicable)			6	13	ns
t_{PHL}	from Clear to output Q (as applicable)			12	24	
t_{PLH}	from Clock			14	21	ns
t_{PHL}	to output Q or $\bar{Q}$			22	27	

Pin Assignments (Top View)
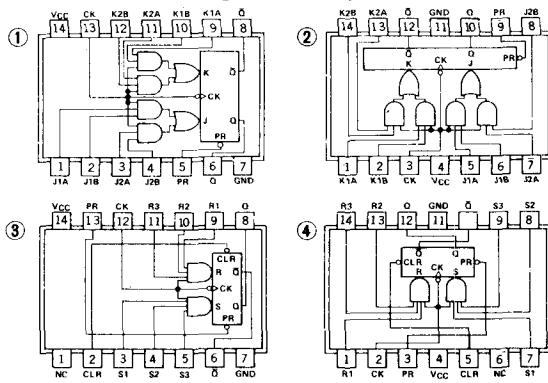
Function Tables

H71 (See Note 2)

INPUTS				OUTPUTS	
PRESET	CLOCK	J	K	Q	$\bar{Q}$
L	X	X	X	H	L
H	⊓	L	L	Q_0	$\bar{Q}_0$
H	⊓	H	L	H	L
H	⊓	L	H	L	H
H	⊓	H	H	TOGGLE	

positive logic: J = (J1A·J1B)×(J2A·J2B)
K = (K1A·K1B)+(K2A·K2B)

L71 (See Note 2)

INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	S	R	Q	$\bar{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	⊓	L	L	Q_0	$\bar{Q}_0$
H	H	⊓	H	L	H	L
H	H	⊓	L	H	L	H
H	H	⊓	H	H	INDETERMINATE	

positive logic: R = R1·R2·R3
S = S1·S2·S3

Functional Block Diagrams

H71-GATED J-K WITH PRESET

L71-GATED R-S WITH AND PRESET ESET
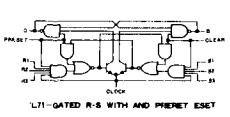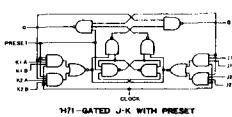
NOTES: 1 : with all outputs open, I_{CC} is measured with the Q and $\bar{Q}$ outputs high in turn. At the time of measurement, the clock input is grounded.
2 : H = high level (steady state). L = low level (steady state). X = irrelevant
⊓ = high-level pulse, data inputs shouts be held constant while clock is high; data is transferred to output on the falling edge of the pulse.
Qo = the level of Q before the indicated input conditions were established.
TOGGLE : Each output changes to the complement of its previous level on each active transition (pulse) of the clock.
▪ This configuration is nonstable; that is, it will not persist when preset and clear inputs return to thurn to their inactive (high) level.

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at $V_{CC}=5V$, $T_A=25°C$.
◆Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.
* t_{PLH} ≡ propagation delay time, low-to-high-level output.
t_{PHL} ≡ propagation delay time, high-to-low-level output.
↑↓The arrow indicates the edge of the clock pulse used for reference: ↑ for the rising edge, ↓ for the falling edge.