intel®

82C284
CLOCK GENERATOR AND READY INTERFACE FOR 80286 PROCESSORS
(82C284-12, 82C284-10, 82C284-8)

- **Generates System Clock for 80286 Processors**
- **Uses Crystal or TTL Signal for Frequency Source**
- **Provides Local READY and MULTIBUSI READY Synchronization**
- **High Speed CHMOS III Technology**
- **Generates System Reset Output**
- **Available in 18-Lead Cerdip and 20-Pin PLCC (Plastic Leaded Chip Carrier) Packages**
  (See Packaging Spec. Order #231369)

The 82C284 is a clock generator/driver which provides clock signals for 80286 processors and support components. It also contains logic to supply $\overline{\text{READY}}$ to the CPU from either asynchronous or synchronous sources and synchronous RESET from an asynchronous input.

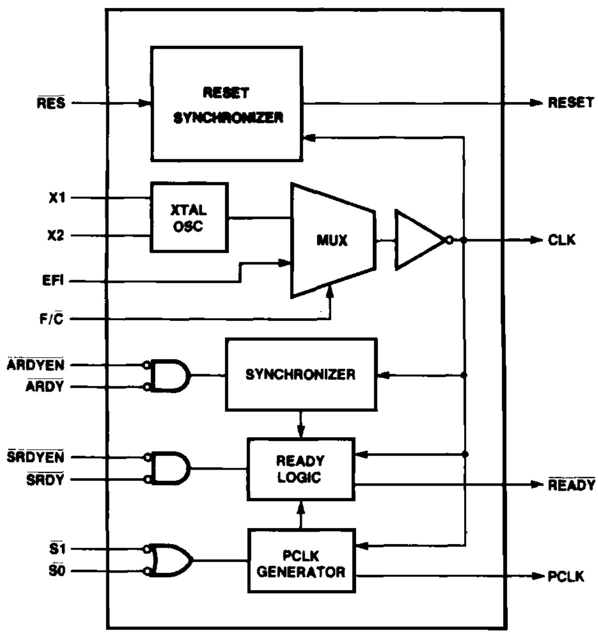
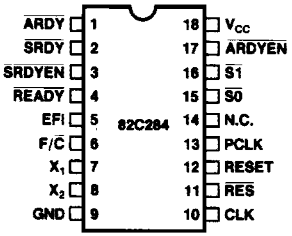


Figure 1. 82C284 Block Diagram

October 1990
Order Number: 210453-011

18-Lead Cerdip



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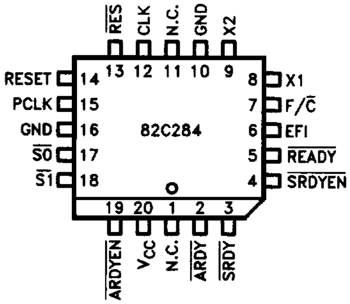
P.C. Board Views—As viewed from the component side of the P.C. Board.

Component Pad Views—As viewed from underside of component when mounted on the board.

20 Pin PLCC



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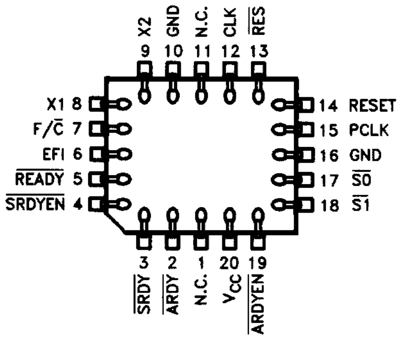

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NOTE:
1. N.C. Signals must not be connected.

Figure 2. 82C284 Pin Configuration

2

Table 1. Pin Description

The following pin function descriptions are for the 82C284 clock generator.

Symbol	Type	Name and Function
CLK	O	**SYSTEM CLOCK** is the signal used by the processor and support devices which must be synchronous with the processor. The frequency of the CLK output has twice the desired internal processor clock frequency. CLK can drive both TTL and MOS level inputs.
F/$\overline{\text{C}}$	I	**FREQUENCY/CRYSTAL SELECT** is a strapping option to select the source for the CLK output. When F/$\overline{\text{C}}$ is strapped LOW, the internal crystal oscillator drives CLK. When F/$\overline{\text{C}}$ is strapped HIGH, the EFI input drives the CLK output.
X1, X2	I	**CRYSTAL IN** are the pins to which a parallel resonant fundamental mode crystal is attached for the internal oscillator. When F/$\overline{\text{C}}$ is LOW, the internal oscillator will drive the CLK output at the crystal frequency. The crystal frequency must be twice the desired internal processor clock frequency.
EFI	I	**EXTERNAL FREQUENCY IN** drives CLK when the F/$\overline{\text{C}}$ input is strapped HIGH. The EFI input frequency must be twice the desired internal processor clock frequency.
PCLK	O	**PERIPHERAL CLOCK** is an output which provides a 50% duty cycle clock with 1/2 the frequency of CLK. PCLK will be in phase with the internal processor clock following the first bus cycle after the processor has been reset.
$\overline{\text{ARDYEN}}$	I	**ASYNCHRONOUS READY ENABLE** is an active LOW input which qualifies the $\overline{\text{ARDY}}$ input. $\overline{\text{ARDYEN}}$ selects $\overline{\text{ARDY}}$ as the source of ready for the current bus cycle. Inputs to $\overline{\text{ARDYEN}}$ may be applied asynchronously to CLK. Setup and hold times are given to assure a guaranteed response to synchronous inputs.
$\overline{\text{ARDY}}$	I	**ASYNCHRONOUS READY** is an active LOW input used to terminate the current bus cycle. The $\overline{\text{ARDY}}$ input is qualified by $\overline{\text{ARDYEN}}$. Inputs to $\overline{\text{ARDY}}$ may be applied asynchronously to CLK. Setup and hold times are given to assure a guaranteed response to synchronous outputs.
$\overline{\text{SRDYEN}}$	I	**SYNCHRONOUS READY ENABLE** is an active LOW input which qualifies $\overline{\text{SRDY}}$. $\overline{\text{SRDYEN}}$ selects $\overline{\text{SRDY}}$ as the source for $\overline{\text{READY}}$ to the CPU for the current bus cycle. Setup and hold times must be satisfied for proper operation.
$\overline{\text{SRDY}}$	I	**SYNCHRONOUS READY** is an active LOW input used to terminate the current bus cycle. The $\overline{\text{SRDY}}$ input is qualified by the $\overline{\text{SRDYEN}}$ input. Setup and hold times must be satisfied for proper operation.
$\overline{\text{READY}}$	O	**READY** is an active LOW output which signals the current bus cycle is to be completed. The $\overline{\text{SRDY}}$, $\overline{\text{SRDYEN}}$, $\overline{\text{ARDY}}$, $\overline{\text{ARDYEN}}$, $\overline{\text{S1}}$, $\overline{\text{S0}}$ and $\overline{\text{RES}}$ inputs control $\overline{\text{READY}}$ as explained later in the $\overline{\text{READY}}$ generator section. $\overline{\text{READY}}$ is an open drain output requiring an external pull-up resistor.

Table 1. Pin Description (Continued)

The following pin function descriptions are for the 82C284 clock generator.

Symbol	Type	Name and Function
$\overline{S0}$, $\overline{S1}$	I	**STATUS** input prepare the 82C284 for a subsequent bus cycle. $\overline{S0}$ and $\overline{S1}$ synchronize PCLK to the internal processor clock and control $\overline{READY}$. These inputs have internal pull-up resistors to keep them HIGH if nothing is driving them. Setup and hold times must be satisfied for proper operation.
RESET	O	**RESET** is an active HIGH output which is derived from the $\overline{RES}$ input. RESET is used to force the system into an initial state. When RESET is active, $\overline{READY}$ will be active (LOW).
$\overline{RES}$	I	**RESET IN** is an active LOW input which generates the system reset signal, RESET. Signals to $\overline{RES}$ may be applied asynchronously to CLK. Setup and hold times are given to assure a guaranteed response to synchronous inputs.
V_{CC}		**SYSTEM POWER:** +5V Power Supply
GND		**SYSTEM GROUND:** 0V

2

FUNCTIONAL DESCRIPTION

Introduction

The 82C284 generates the clock, ready, and reset signals required for 80286 processors and support components. The 82C284 contains a crystal controlled oscillator, clock generator, peripheral clock generator, Multibus ready synchronization logic and system reset generation logic.

Clock Generator

The CLK output provides the basic timing control for an 80286 system. CLK has output characteristics sufficient to drive MOS devices. CLK is generated by either an internal crystal oscillator or an external source as selected by the F/$\overline{C}$ strapping option. When F/$\overline{C}$ is LOW, the crystal oscillator drives the CLK output. When F/$\overline{C}$ is HIGH, the EFI input drives the CLK output.

The 82C284 provides a second clock output, PCLK, for peripheral devices. PCLK is CLK divided by two. PCLK has a duty cycle of 50% and MOS output drive characteristics. PCLK is normally synchronized to the internal processor clock.

After reset, the PCLK signal may be out of phase with the internal processor clock. The $\overline{S1}$ and $\overline{S0}$ signals of the first bus cycle are used to synchronize PCLK to the internal processor clock. The phase of the PCLK output changes by extending its HIGH time beyond one system clock (see waveforms). PCLK is forced HIGH whenever either $\overline{S0}$ or $\overline{S1}$ were active (LOW) for the two previous CLK cycles. PCLK continues to oscillate when both $\overline{S0}$ and $\overline{S1}$ are HIGH.

Since the phase of the internal processor clock will not change except during reset, the phase of PCLK will not change except during the first bus cycle after reset.

Oscillator

The oscillator circuit of the 82C284 is a linear Pierce oscillator which requires an external parallel resonant, fundamental mode, crystal. The output of the oscillator is internally buffered. The crystal frequency chosen should be twice the required internal processor clock frequency. The crystal should have a typical load capacitance of 32 pF.

X1 and X2 are the oscillator crystal connections. For stable operation of the oscillator, two loading capacitors are recommended, as shown in Table 2. The sum of the board capacitance and loading capacitance should equal the values shown. It is advisable to limit stray board capacitances (not including the effect of the loading capacitors or crystal capacitance) to less than 10 pF between the X1 and X2 pins. Decouple V_{CC} and GND as close to the 82C284 as possible.

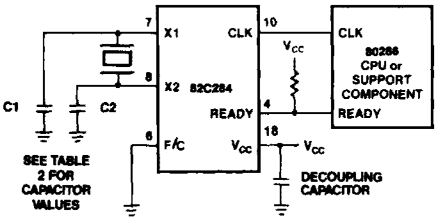


Figure 3. Recommended Crystal and $\overline{\text{READY}}$ Connections

CLK Termination

Due to the CLK output having a very fast rise and fall time, it is recommended to properly terminate the CLK line at frequencies above 10 MHz to avoid signal reflections and ringing. Termination is accomplished by inserting a small resistor (typically 10Ω–74Ω) in series with the output, as shown in Figure 4. This is known as series termination. The resistor value plus the circuit output impedance should be made equal to the impedance of the transmission line.

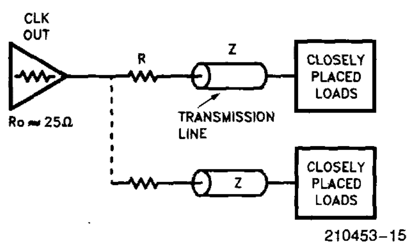


Figure 4. Series Termination

Reset Operation

The reset logic provides the RESET output to force the system into a known, initial state. When the $\overline{\text{RES}}$ input is active (LOW), the RESET output becomes active (HIGH). $\overline{\text{RES}}$ is synchronized internally at the falling edge of CLK before generating the RESET output (see waveforms). Synchronization of the $\overline{\text{RES}}$ input introduces a one or two CLK delay before affecting the RESET output.

At power up, a system does not have a stable V_{CC} and CLK. To prevent spurious activity, $\overline{\text{RES}}$ should be asserted until V_{CC} and CLK stabilize at their operating values. 80286 processors and support components also require their RESET inputs be HIGH a minimum of 16 CLK cycles. A network such as shown in Figure 5 will keep $\overline{\text{RES}}$ LOW long enough to satisfy both needs.

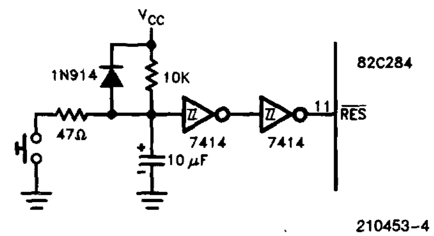


Figure 5. Typical $\overline{\text{RES}}$ Timing Circuit

Ready Operation

The 82C284 accepts two ready sources for the system ready signal which terminates the current bus cycle. Either a synchronous ($\overline{\text{SRDY}}$) or asynchronous ready ($\overline{\text{ARDY}}$) source may be used. Each ready input has an enable ($\overline{\text{SRDYEN}}$ and $\overline{\text{ARDYEN}}$) for selecting the type of ready source required to terminate the current bus cycle. An address decoder would normally select one of the enable inputs.

$\overline{\text{READY}}$ is enabled (LOW), if either $\overline{\text{SRDY}}$ + $\overline{\text{SRDYEN}}$ = 0 or $\overline{\text{ARDY}}$ + $\overline{\text{ARDYEN}}$ = 0 when sampled by the 82C284 $\overline{\text{READY}}$ generation logic. $\overline{\text{READY}}$ will remain active for at least two CLK cycles.

The $\overline{\text{READY}}$ output has an open-drain driver allowing other ready circuits to be wire or'ed with it, as shown in Figure 3. The $\overline{\text{READY}}$ signal of an 80286 system requires an external pull-up resistor. To force the $\overline{\text{READY}}$ signal inactive (HIGH) at the start of a bus cycle, the $\overline{\text{READY}}$ output floats when either $\overline{\text{S1}}$ or $\overline{\text{S0}}$ are sampled LOW at the falling edge of CLK. Two system clock periods are allowed for the pull-up resistor to pull the $\overline{\text{READY}}$ signal to V_{IH}. When RESET is active, $\overline{\text{READY}}$ is forced active one CLK later (see waveforms).

Figure 6 illustrates the operation of $\overline{\text{SRDY}}$ and $\overline{\text{SRDYEN}}$. These inputs are sampled on the falling edge of CLK when $\overline{\text{S1}}$ and $\overline{\text{S0}}$ are inactive and PCLK is HIGH. $\overline{\text{READY}}$ is forced active when both $\overline{\text{SRDY}}$ and $\overline{\text{SRDYEN}}$ are sampled as LOW.

Figure 7 shows the operation of $\overline{\text{ARDY}}$ and $\overline{\text{ARDYEN}}$. These inputs are sampled by an internal synchronizer at each falling edge of CLK. The output of the synchronizer is then sampled when PCLK is HIGH. If the synchronizer resolved both the $\overline{\text{ARDY}}$ and $\overline{\text{ARDYEN}}$ as active, the $\overline{\text{SRDY}}$ and $\overline{\text{SRDYEN}}$ inputs are ignored. Either $\overline{\text{ARDY}}$ or $\overline{\text{ARDYEN}}$ must be HIGH at the end of T_S (see Figure 7).

$\overline{\text{READY}}$ remains active until either $\overline{\text{S1}}$ or $\overline{\text{S0}}$ are sampled LOW, or the ready inputs are sampled as inactive.

Table 2. 82C284 Crystal Loading Capacitance Values

Crystal Frequency	C1 Capacitance (Pin 7)	C2 Capacitance (Pin 8)
1 to 8 MHz	60 pF	40 pF
8 to 20 MHz	25 pF	15 pF
Above 20 MHz	15 pF	15 pF

NOTE:
Capacitance values must include stray board capacitance.

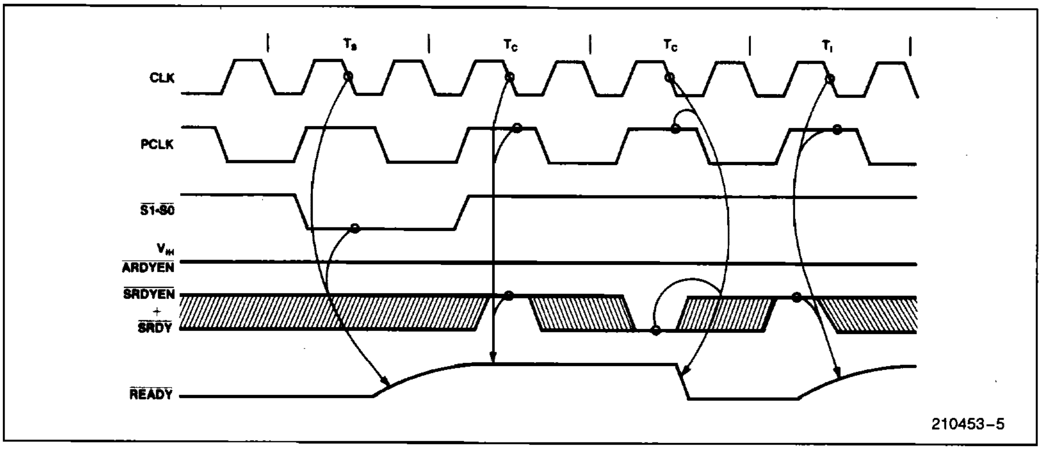


Figure 6. Synchronous Ready Operation

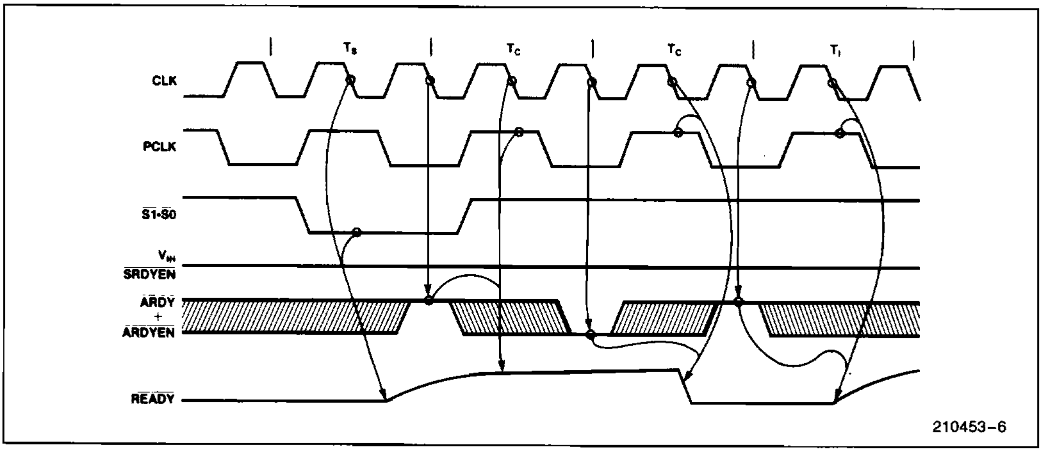


Figure 7. Asynchronous Ready Operation

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias .... 0°C to +70°C
Storage Temperature .... −65°C to +150°C
All Output and Supply Voltages ..... −0.5V to +7V
All Input Voltages .... −1.0V to +5.5V
Power Dissipation .... 1 Watt

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

D.C. CHARACTERISTICS T_{CASE} = 0°C to +85°C,* V_{CC} = 5V ±5%

Symbol	Parameter	Min	Max	Unit	Test Condition
V_{IL}	Input LOW Voltage		0.8	V	
V_{IH}	Input HIGH Voltage	2.0		V	
V_{IHR}	$\overline{RES}$ and EFI Input HIGH Voltage	2.6		V	
V_{OL}	RESET, PCLK Output LOW Voltage		0.45	V	I_{OL} = 5 mA
V_{OH}	RESET, PCLK Output HIGH Voltage	2.4		V	I_{OH} = −1 mA
		V_{CC}−0.5		V	I_{OH} = −0.2 mA
V_{OLR}	$\overline{READY}$, Output LOW Voltage		0.45	V	I_{OL} = 9 mA
V_{OLC}	CLK Output LOW Voltage		0.45	V	I_{OL} = 5 mA
V_{OHC}	CLK Output HIGH Voltage	4.0		V	I_{OH} = − 800 μA
I_{IL}	Input Sustaining Current on $\overline{S0}$ and $\overline{S1}$ Pins	−60	−500	μA	V_{IN} = 0V
I_{LI}	Input Leakage Current		±10	μA	$0 \leq V_{IN} \leq V_{CC}$(1)
I_{CC}	Power Supply Current		75	mA	at 25 MHz Output CLK Frequency
C_I	Input Capacitance		10	pF	F_C = 1 MHz

*T_A is guaranteed from 0°C to +70°C as long as T_{CASE} is not exceeded.

NOTE:
1. Status lines S0 and S1 excluded because they have internal pull-up resistors.

A.C. CHARACTERISTICS V_{CC} = 5V ±5%, T_{CASE} = 0°C to +85°C.*

Timings are referenced to 0.8V and 2.0V points of signals as illustrated in the datasheet waveforms, unless otherwise noted.

82C284 A.C. Timing Parameters

Symbol	Parameter	8 MHz		10 MHz		12.5 MHz		Units	Test Conditions
		Min	Max	Min	Max	Min	Max		
1	EFI to CLK Delay		25		25		25	ns	At 1.5V (1)
2	EFI LOW Time	28		22.5		13		ns	At 1.5V (1, 7)
3	EFI HIGH Time	28		22.5		22		ns	At 1.5V (1, 7)
4	CLK Period	62	500	50	500	40	500	ns	
5	CLK LOW Time	15		12		11		ns	At 1.0V (1, 2, 7, 8, 9, 10)
6	CLK HIGH Time	25		16		13		ns	At 3.6V (1, 2, 7, 8, 9, 10)
7	CLK Rise Time		10		8		8	ns	1.0V to 3.6V (1, 2, 10, 11)
8	CLK Fall Time		10		8		8	ns	3.6V to 1.0V (1, 9, 10, 11)
9	Status Setup Time	22		—		—		ns	(Note 1)
9a	Status Setup Time for Status Going Active	—		20		22		ns	(Note 1)
9b	Status Setup Time for Status Going Inactive	—		20		18		ns	(Note 1)
10	Status Hold Time	1		1		3		ns	(Note 1)
11	$\overline{SRDY}$ or $\overline{SRDYEN}$ Setup Time	20		17.5		17		ns	(Note 1)
12	$\overline{SRDY}$ or $\overline{SRDYEN}$ Hold Time	0		2		2		ns	(Notes 1, 11)
13	$\overline{ARDY}$ or $\overline{ARDYEN}$ Setup Time	0		0		0		ns	(Notes 1, 3)
14	$\overline{ARDY}$ or $\overline{ARDYEN}$ Hold Time	30		30		25		ns	(Notes 1, 3)
15	$\overline{RES}$ Setup Time	20		20		18		ns	(Notes 1, 3)
16	$\overline{RES}$ Hold Time	10		10		8		ns	(Notes 1, 3)
17	$\overline{READY}$ Inactive Delay	5		5		5		ns	At 0.8V (4)
18	$\overline{READY}$ Active Delay	0	24	0	24	0	18	ns	At 0.8V (4)
19	PCLK Delay	0	45	0	35	0	23	ns	(Note 5)
20	RESET Delay	5	34	5	27	3	22	ns	(Note 5)
21	PCLK LOW Time	t4−20		t4−20		t4−20		ns	(Notes 5, 6)
22	PCLK HIGH Time	t4−20		t4−20		t4−20		ns	(Notes 5, 6)

*T_A is guaranteed from 0°C to 70°C as long as T_{CASE} is not exceeded.

NOTES:

1. CLK loading: C_L = 100 pF. The 82C284's X1 and X2 inputs are designed primarily for parallel-resonant crystals. Serial-resonant crystals may also be used, however, they may oscillate up to 0.01% faster than their nominal frequencies when used with the 82C284. For either type of crystal, capacitive loading should be as specified by Table 2.
2. With the internal crystal oscillator using recommended crystal and capacitive loading; or with the EFI input meeting specifications t2 and t3. The recommended crystal loading for CLK frequencies of 8 MHz–20 MHz are 25 pF from pin X_1 to ground, and 15 pF from pin X_2 to ground; for CLK frequencies above 20 MHz 15 pF from pin X_1 to ground, and 15 pF from pin X_2 to ground. These recommended values are ±5 pF and include all stray capacitance. Decouple V_{CC} and GND as close to the 82C284 as possible.
3. This is an asynchronous input. This specification is given for testing purposes only, to assure recognition at specific CLK edge.

NOTES:

4. Pull-up Resistor values for READY Pin:

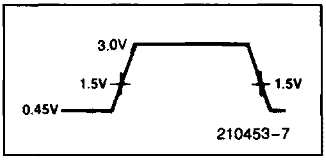
CPU Frequency	8 MHz	10 MHz	12.5 MHz
Resistor	910Ω	700Ω	600Ω
CL	150 pF	150 pF	150 pF
I_{OL}	7 mA	7 mA	9 mA

5. PCLK and RESET loading: C_L = 75 pF.
6. t4 refers to any allowable CLK period.
7. When driving the 82C284 with EFI, provide minimum EFI HIGH and LOW times as follows:

CLK Output Frequency	16 MHz	20 MHz	25 MHz
Min. Required EFI HIGH Time	28 ns	22.5 ns	22 ns
Min. Required EFI LOW Time	28 ns	22.5 ns	13 ns

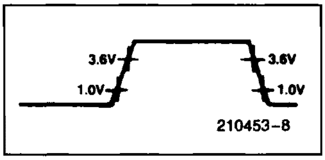
8. When using a crystal (with recommended capacitive loading per Table 2) appropriate for the speed of the 80286, CLK output HIGH and LOW times guaranteed to meet the 80286 requirements.

Reset Drive EFI Drive and Measurement Points



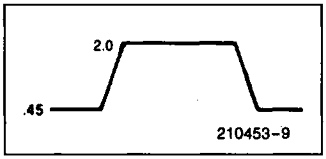
Note 9

CLK Output Measurement Points

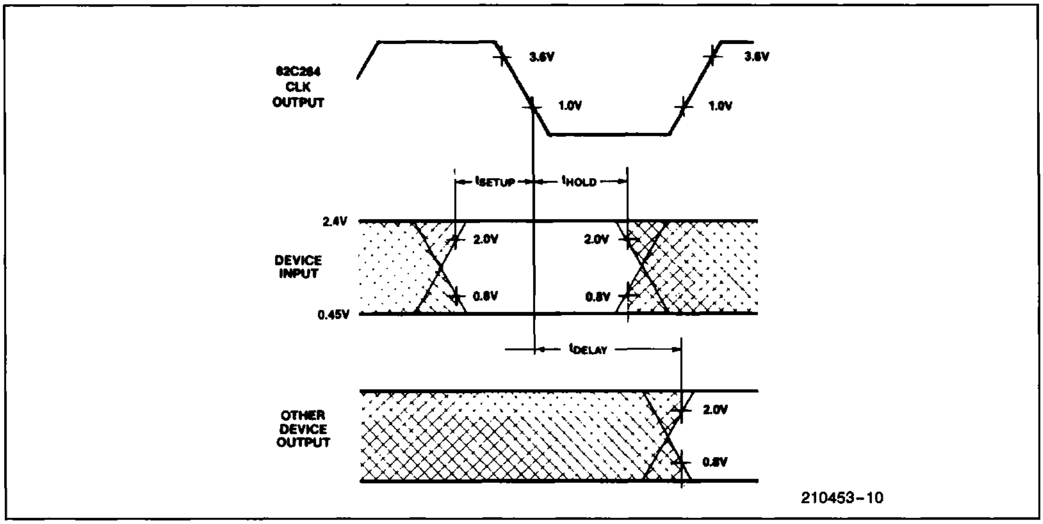


Note 10

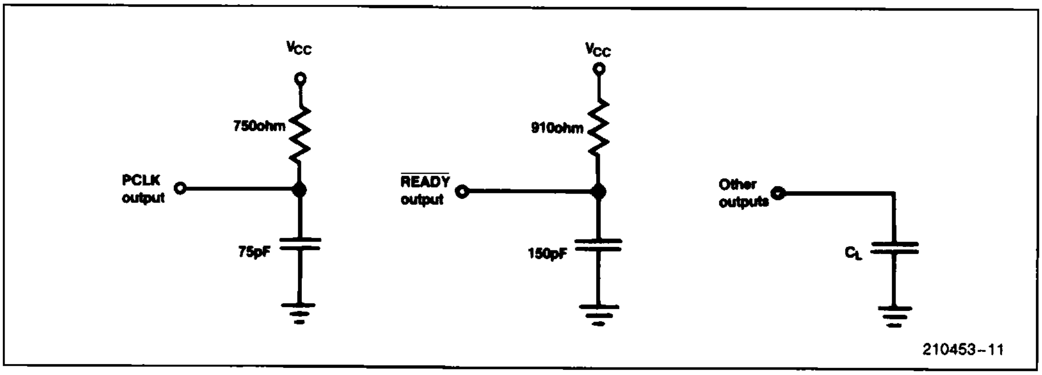
F/$\overline{C}$ Drive Points



Note 11



Note 12. AC Setup, Hold and Delay Time Measurement—General



Note 13. AC Test Loading on Outputs

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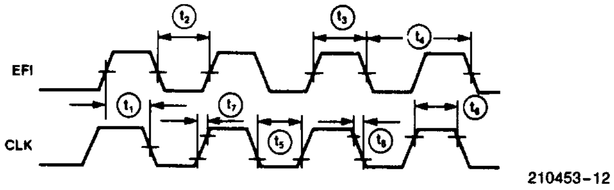
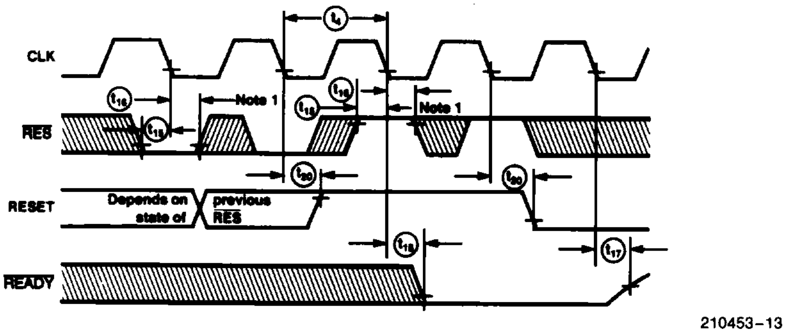
WAVEFORMS

CLK as a Function of EFI



NOTE:
The EFI input LOW and HIGH times as shown are required to guarantee the CLK LOW and HIGH times shown.

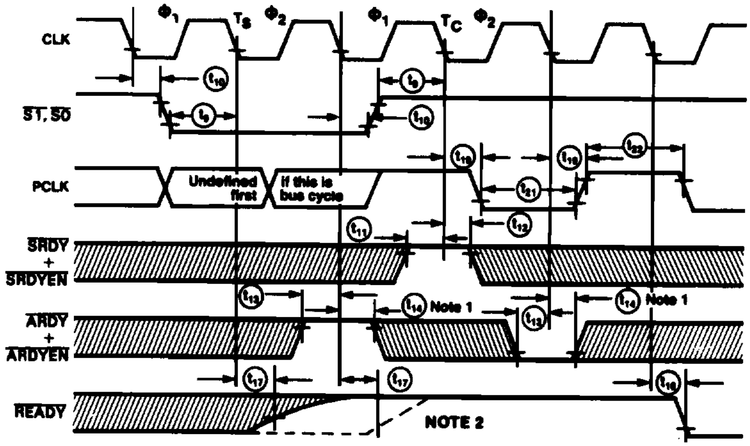
RESET and READY Timing as a Function of RES with S1, S0, ARDY + ARDYEN, and SRDY + SRDYEN High



NOTE:
1. This is an asynchronous input. The setup and hold times shown are required to guarantee the response shown.

WAVEFORMS (Continued)

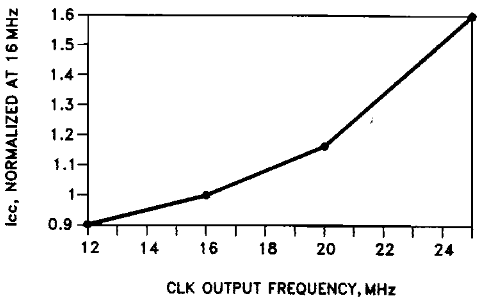
READY and PCLK Timing with RES High



210453-14

NOTES:
1. This is an asynchronous input. The setup and hold times shown are required to guarantee the response shown.
2. If $\overline{SRDY}$ + $\overline{SRDYEN}$ or $\overline{ARDY}$ + $\overline{ARDYEN}$ are active before and/or during the first bus cycle after RESET, $\overline{READY}$ may not be deasserted until after the falling edge of $\phi 2$ of T_S.

I_{CC} vs Frequency @ Nominal Conditions



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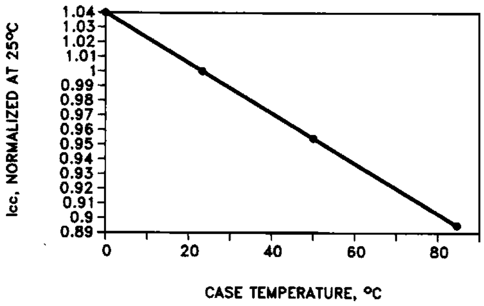
I_{CC} vs Case Temperature @ 25 MHz



2310453-17

DATA SHEET REVISION REVIEW

The following list represents key differences between this and the -010 data sheet. Please review this summary carefully.

1. The DC Characteristics Input Sustaining Current on $\overline{S}_0$ and $\overline{S}_1$ pins (I_{IL}) has been changed from $-30\ \mu A$ to $-60\ \mu A$.
2. The AC Timing parameter $\overline{SRDY}$ or $\overline{SRDYEN}$ setup time (t_{11}) has been changed to 17.5 ns for the 10 MHz and 17 ns for the 12.5 MHz parts.