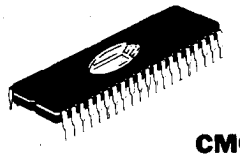


M5M27C402K-12,- 15

4194304-BIT(262144-WORD BY 16-BIT) CMOS ERASABLE AND ELECTRICALLY REPROGRAMMABLE ROM

DESCRIPTION

The Mitsubishi M5M27C402K is a high-speed 4194304-bit ultraviolet erasable and electrically reprogrammable read only memory. It is suitable for microprocessor programming applications where rapid turn-around is required. The M5M27C402K is fabricated by N-channel double polysilicon gate for Memory and CMOS technology for peripheral circuits, and is available in a 40 pin DIP with a transparent lid.

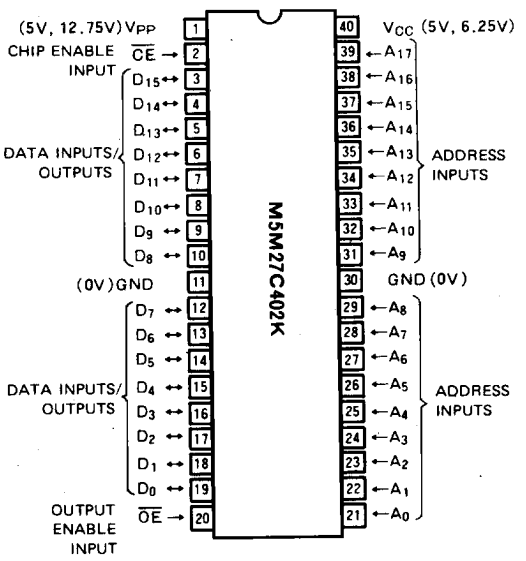
FEATURES

- 262144 word x 16 bit organization
- Access time M5M27C402K-12 . . . . . 120ns (max)
  M5M27C402K-15 . . . . . 150ns (max)
- Two line control $\overline{OE}$, $\overline{CE}$
- Low power current (I_{CC}): Active . . . . . 30mA (max)
  (I_{SB2}): Stand by . . . 0.1mA (max)
- Single 5V power supply
- Programming voltage 12.75V
- 3-State output buffer
- Input and outut TTL-compatible in read and program mode
- Standard 40 pin DIP
- Word programming algorithm

APPLICATION

Microcomputer systems and peripheral equipment

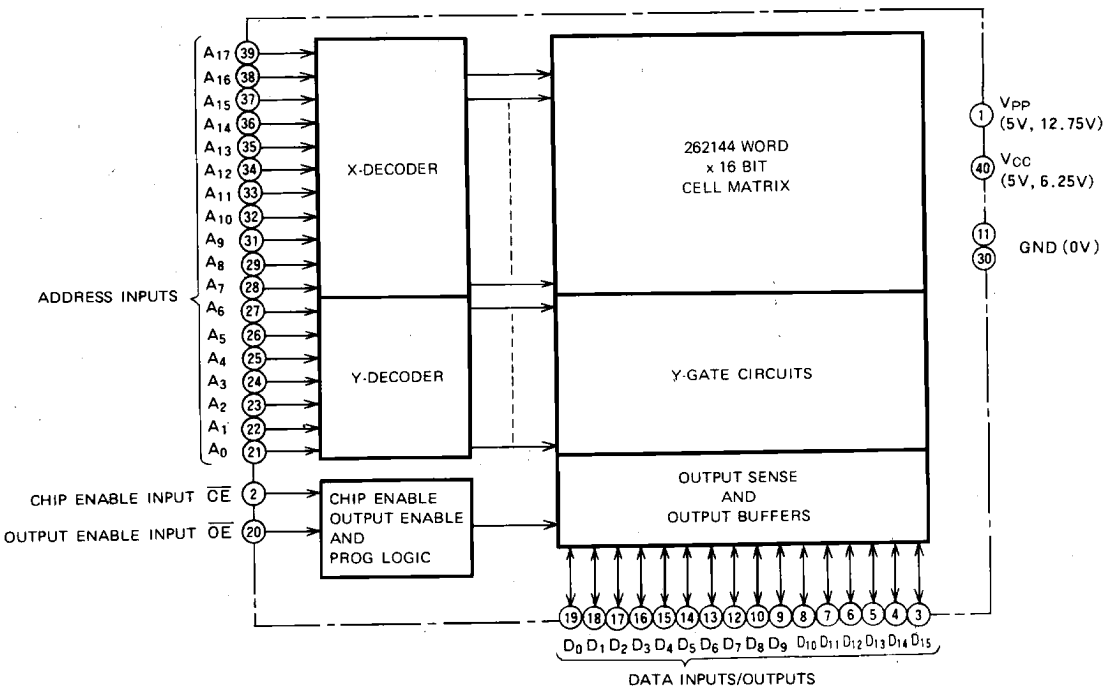
PIN CONFIGURATION (TOP VIEW)



NC: NO CONNECTION

Outline 40K4

BLOCK DIAGRAM



4194304-BIT(262144-WORD BY 16-BIT) CMOS ERASABLE AND ELECTRICALLY REPROGRAMMABLE ROM

FUNCTION

Read

Set the $\overline{CE}$ and $\overline{OE}$ terminals to the read mode (low level). Low level input to $\overline{CE}$ and $\overline{OE}$ and address signals to the address inputs ($A_0 \sim A_{17}$) make the data contents of the designated address location available at the data input/output ($D_0 \sim D_{15}$). When the $\overline{CE}$ or $\overline{OE}$ signal is high, data input/output are in a floating state.

When the $\overline{CE}$ signal is high, the device is in the stand by mode or power-down mode.

Programming (Word programming algorithm)

The M5M27C402K enters the word programming mode when 12.75V is supplied to the V_{PP} power supply input, and $\overline{OE}$ is at high level. A location is designated by address signals ($A_0 \sim A_{17}$), and the data to be programmed must be applied at 16-bits in parallel to the data inputs ($D_0 \sim D_{15}$).

Erase

Erase is effected by exposure to ultraviolet light with a wavelength of 2537Å at an intensity of approximately 15WS/cm^2. Sunlight and fluorescent light may contain ultraviolet light sufficient to erase the programmed information. For any operation in the read mode, the transparent lid should be covered with opaque tape.

MODE SELECTION

Mode \ Pins	$\overline{CE}$ (2)	$\overline{OE}$ (20)	V_{PP} (1)	V_{CC} (40)	Data I/O (3~10, 12~19)
Read	V_{IL}	V_{IL}	5V	5V	Data out
Output disable	V_{IL}	V_{IH}	5V	5V	Floating
Standby (Power down)	V_{IH}	X *	5V	5V	Floating
Word program	V_{IL}	V_{IH}	12.75V	6.25V	Data in
Program verify	V_{IH}	V_{IL}	12.75V	6.25V	Data out
Program inhibit	V_{IH}	V_{IH}	12.75V	6.25V	Floating

* : X can be either V_{IL} or V_{IH}.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Symbol	Parameter	Test condition	Ratings	Unit
V_{I1}	All input or output voltage except V_{PP}, A_9	With respect to Ground	−0.6~7	V
V_{I2}	V_{PP} supply voltage		−0.6~14.0	V
V_{I3}	A_9 supply voltage		−0.6~13.5	V
Topr	Operating temperature		−10~80	°C
Tstg	Storage temperature		−65~125	°C

Note 1: Stresses above those listed may cause parmanent damage to the device. This is a stress rating only and functional operation of the device at those or at any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods affects device reliability.

4194304-BIT(262144-WORD BY 16-BIT) CMOS ERASABLE AND ELECTRICALLY REPROGRAMMABLE ROM

READ OPERATION

DC ELECTRICAL CHARACTERISTICS (T_a=0~70°C, V_{CC}=5V±10%, V_{PP}=V_{CC}, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
I_{LI}	Input load current	V_{IN}=0~V_{CC}			10	μA
I_{LO}	Output leakage current	V_{OUT}=0~V_{CC}			10	μA
I_{PP1}	V_{PP} current read	V_{PP}=V_{CC}=5.5V		1	100	μA
I_{SB1}	V_{CC} current standby	$\overline{CE}$=V_{IH}			1	mA
I_{SB2}		$\overline{CE}$=V_{CC}		1	100	μA
I_{CC1}	V_{CC} current Active	$\overline{CE}$=$\overline{OE}$=V_{IL}			30	mA
I_{CC2}		f=8.33MHz, I_{OUT}=0mA			30	mA
V_{IL}	Input low voltage		−0.1		0.8	V
V_{IH}	Input high voltage		2.2		V_{CC}+1	V
V_{OL}	Output low voltage	I_{OL}=2.1mA			0.45	V
V_{OH}	Output high voltage	I_{OH}=−400μA	2.4			V

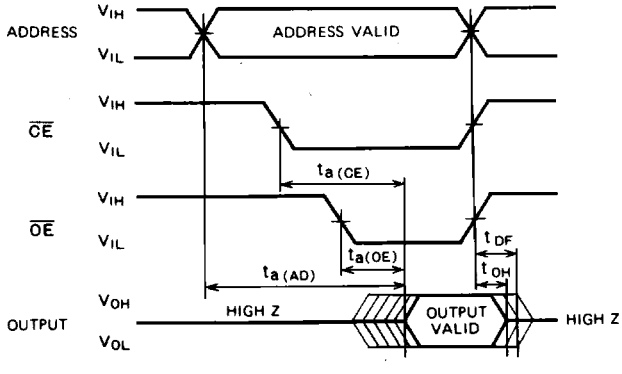
Note 2: Typical values are at T_a = 25°C and nominal supply voltages.

AC ELECTRICAL CHARACTERISTICS (T_a=0~70°C, V_{CC}=5V±10%, V_{PP}=V_{CC}, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits				Unit
			M5M27C402K-12		M5M27C402K-15		
			Min	Max	Min	Max	
$t_{a(AD)}$	Address to output delay	$\overline{CE}$=$\overline{OE}$=V_{IL}		120		150	ns
$t_{a(CE)}$	$\overline{CE}$ to output delay	$\overline{OE}$=V_{IL}		120		150	ns
$t_{a(OE)}$	$\overline{OE}$ to output delay	$\overline{CE}$=V_{IL}		60		60	ns
t_{DF}	$\overline{OE}$ high to output float	$\overline{CE}$=V_{IL}	0	50	0	50	ns
t_{OH}	Output hold from $\overline{CE}$ or $\overline{OE}$		0		0		ns

Note 3: V_{CC} must be applied simultaneously V_{PP} and removed simultaneously V_{PP}.

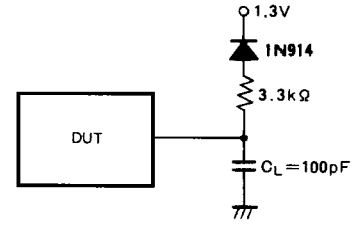
AC WAVEFORMS



Test conditions for A.C. characteristics
Input voltage: V_{IL} = 0.45V, V_{IH} = 2.4V
Input rise and fall times: ≦ 10ns
Reference voltage at timing measurement: 1.5V

Output load: 1TTL gate + C_L (100pF)

or



CAPACITANCE

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
C_{IN}	Input capacitance (Address, $\overline{CE}$, $\overline{OE}$)	Ta=25°C, f=1MHz, V_I=V_O=0V			15	pF
C_{OUT}	Output capacitance				15	pF

PROGRAM OPERATION

First set V_{CC} = 6.25V, V_{PP} = 12.75V and then set an address to first address to be programmed. After applying 0.1 ms program pulse ($\overline{CE}$) to the address, verify is performed. If the output data of that address is not verified correctly, apply one more 0.1 ms program pulse. The programmer continues 0.1 ms pulse-then-verify routines until the device verify correctly or twenty five of these pulse-then-verify routines have been completed. When the programming procedure above is finished, step to the next address and repeat this procedure till last address to be programmed. When the entire addresses have been programmed completely, all addresses should be verified with V_{CC} = V_{PP} = 5V.

DC ELECTRICAL CHARACTERISTICS (T_a = 25±5°C, V_{CC} = 6.25V±0.25V, V_{PP} = 12.75V±0.25V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
I_{LI}	Input current	V_{IN} = 0~V_{CC}			10	μA
V_{OL}	Output low voltage	I_{OL} = 2.1mA			0.45	V
V_{OH}	Output high voltage	I_{OH} = −400μA	2.4			V
V_{IL}	Input low voltage		−0.1		0.8	V
V_{IH}	Input high voltage		2.2		V_{CC}	V
I_{CC}	V_{CC} supply current				30	mA
I_{PP}	V_{PP} supply current	$\overline{CE}$ = V_{IL}			30	mA

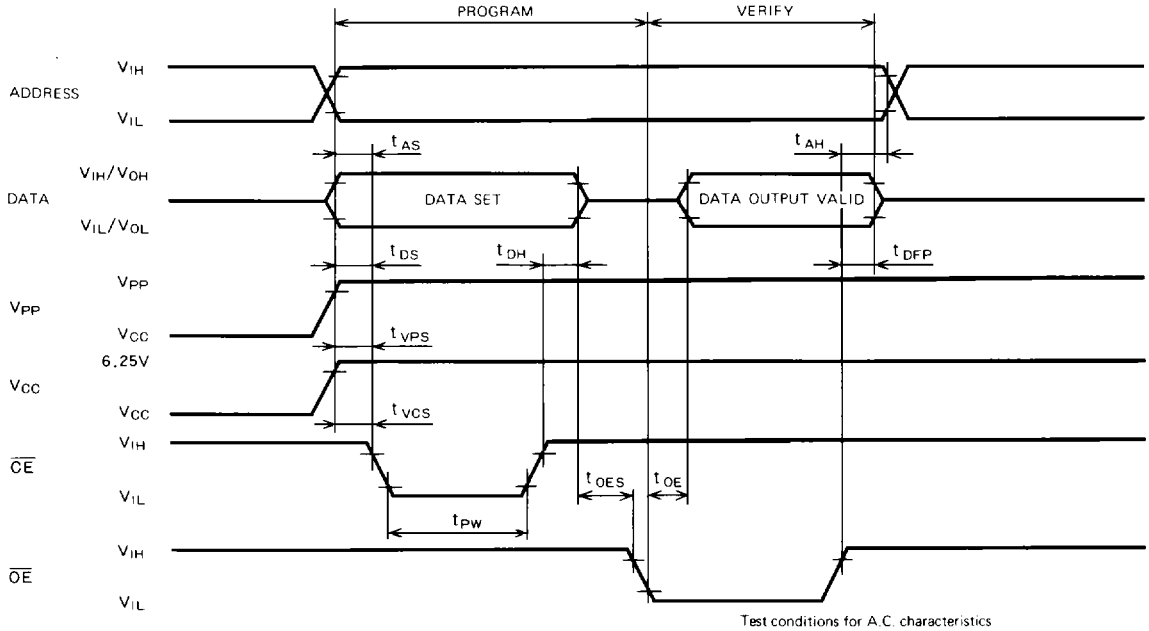
AC ELECTRICAL CHARACTERISTICS (T_a = 25±5°C, V_{CC} = 6.25V±0.25V, V_{PP} = 12.75V±0.25V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{AS}	Address setup time		2			μs
t_{OES}	$\overline{OE}$ set up time		2			μs
t_{DS}	Data setup time		2			μs
t_{AH}	Address hold time		0			μs
t_{DH}	Data hold time		2			μs
t_{DFP}	Chip enable to output float delay		0		130	ns
t_{VCS}	V_{CC} setup time		2			μs
t_{VPS}	V_{PP} setup time		2			μs
t_{PW}	$\overline{CE}$ initial program pulse width		95	100	105	μs
t_{OE}	Data valid from $\overline{OE}$				150	ns

Note 4: V_{CC} must be applied simultaneously V_{PP} and removed simultaneously V_{PP}.

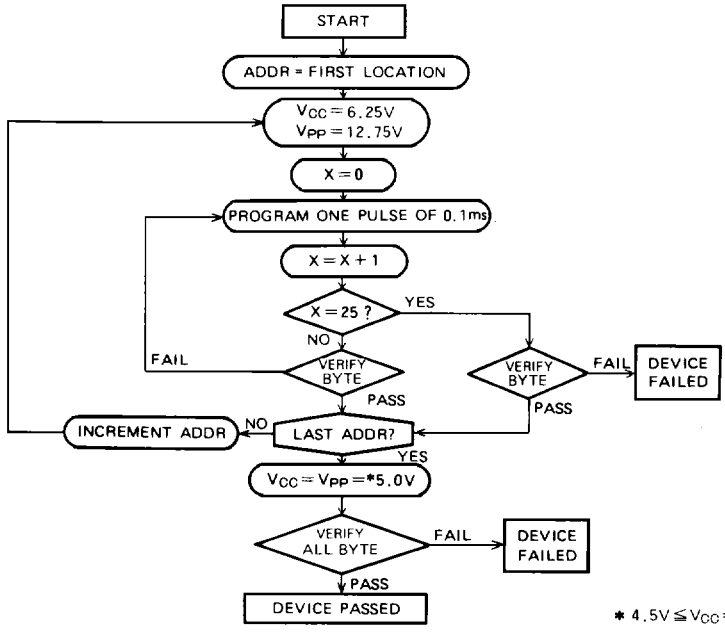
4194304-BIT(262144-WORD BY 16-BIT)
CMOS ERASABLE AND ELECTRICALLY REPROGRAMMABLE ROM

AC WAVEFORMS



Test conditions for A.C. characteristics
Input voltage: V_{IL} = 0.45V, V_{IH} = 2.4V
Input rise and fall times: ≦ 20ns
Reference voltage at timing measurement: Input, Output "L" = 0.8V, "H" = 2V.

PROGRAMMING ALGORITHM FLOW CHART



* 4.5V ≦ V_{CC} = V_{PP} ≦ 5.5V

DEVICE IDENTIFIER MODE

The Device Identifier Mode allows the reading of a binary code from the EPROM that identifies the manufacturer and device type.

The EPROM Programmer reads the manufacturer code and the device code and automatically selects the corresponding programming algorithm.

M5M27C402K DEVICE IDENTIFIER CODE

Code \ Pin	A_0 (21)	D_{15} (3)	D_{14} (4)	D_{13} (5)	D_{12} (6)	D_{11} (7)	D_{10} (8)	D_9 (9)	D_8 (10)	D_7 (12)	D_6 (13)	D_5 (14)	D_4 (15)	D_3 (16)	D_2 (17)	D_1 (18)	D_0 (19)	Hex Data
Manufacturer code	V_{IL}	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	001C
Device code	V_{IH}	0	0	0	0	0	0	0	0	1	0	0	0	1	1	1	1	008F

Note 5: A_9 = 12.0±0.5V.
$A_1 \sim A_8$, $A_{10} \sim A_{17}$, $\overline{CE}$, $\overline{OE}$ = V_{IL}
$V_{CC} = V_{PP} = 5V \pm 10\%$