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LXT6155

155 Mbps SDH/SONET/ATM Transceiver

Datasheet

The LXT6155 is a high speed fully integrated transceiver designed for 155 Mbps SDH/SONET/ ATM transmission system applications. The LXT6155 provides a LVPECL interface for fiber optics modules, and a CMI interface for coax cable drive. These circuits are implemented using Level One's proven low power 3.3V CMOS analog and digital circuits.

The transmitter incorporates a parallel-to-serial converter, a frequency multiplier PLL, CMI line encoders, and line interfaces for both coax cable and optical fiber. The receiver incorporates an adaptive equalizer, a clock recovery PLL, Loss of Signal (LOS) detector, CMI and NRZ decoders, a serial-to-parallel converter, and an SDH/SONET frame byte detector/aligner. At the system interface, the LXT6155 offers both parallel 8-bit and serial differential interfaces. The LXT6155 also operates in either Hardware stand-alone mode or Software mode. Software mode is controlled by a serial microprocessor (μP) to program formats and operating/test modes.

Product Features

Applications

- OC3/STM1 SDH/SONET Cross Connects
- OC3/STM1 SDH/SONET Add/Drop Mux
- OC3/STM1 Transmission Systems
- OC3/STM1 Short Haul Serial Links
- OC3/STM1 ATM/WAN Transmission Systems
- OC3/STM1 ATM/WAN Access Systems

Features

- Complies with:
  —Bellcore SONET GR-253
  —ITU-T G.703/813/958 STM1
- Two line interface formats:
  —Fiber LVPECL NRZ
  —Coax CMI
- Transmit synthesizer PLL

- Receive clock recovery PLL
- Adaptive CMI equalizer
- Analog circuitry for transformer drive
- Programmable LOS function
- CMI encoder and decoder
- Serial/Parallel and Parallel/Serial conversion
- Byte alignment for SDH/SONET frames
- Two modes of operation:
  —Microprocessor controlled; software mode
  —Stand-alone; hardware mode
- No external crystal required. A 19.44 MHz crystal is optional
- Low power consumption (less than 760 mW typical)
- Operates from a single 3.3 V supply
- 64 pin LQFP package

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Revision History

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Figure 1. LXT6155 Block Diagram

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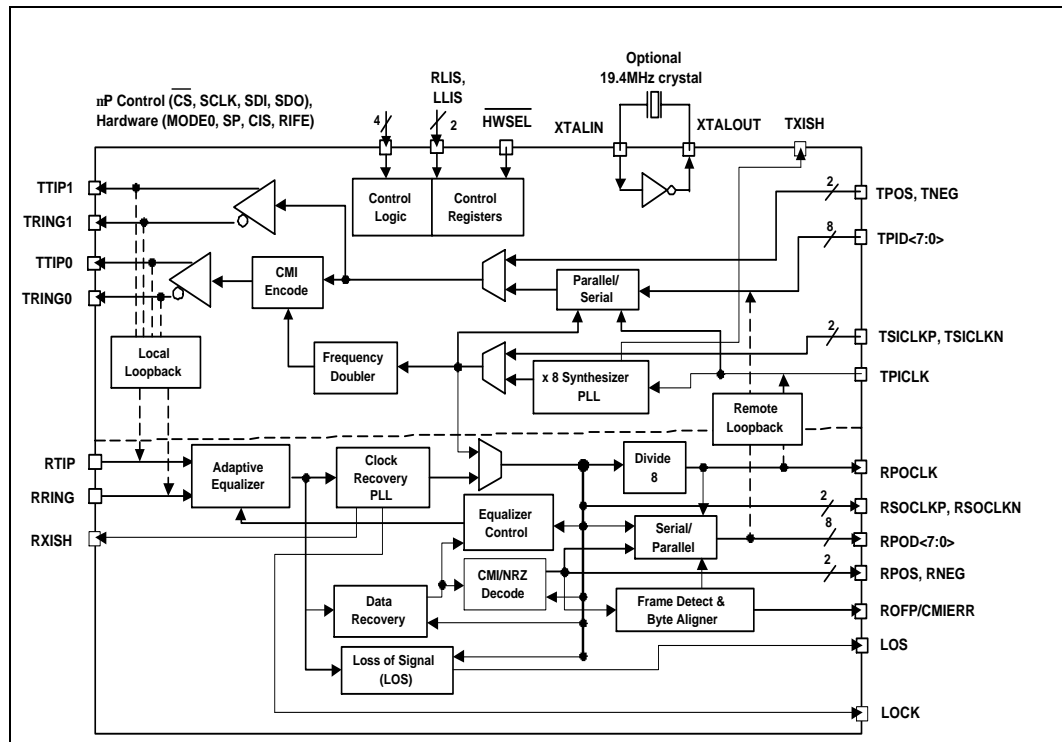
1.0 Pin Assignments and Signal Descriptions

Figure 1. LXT6155 Pin Assignments
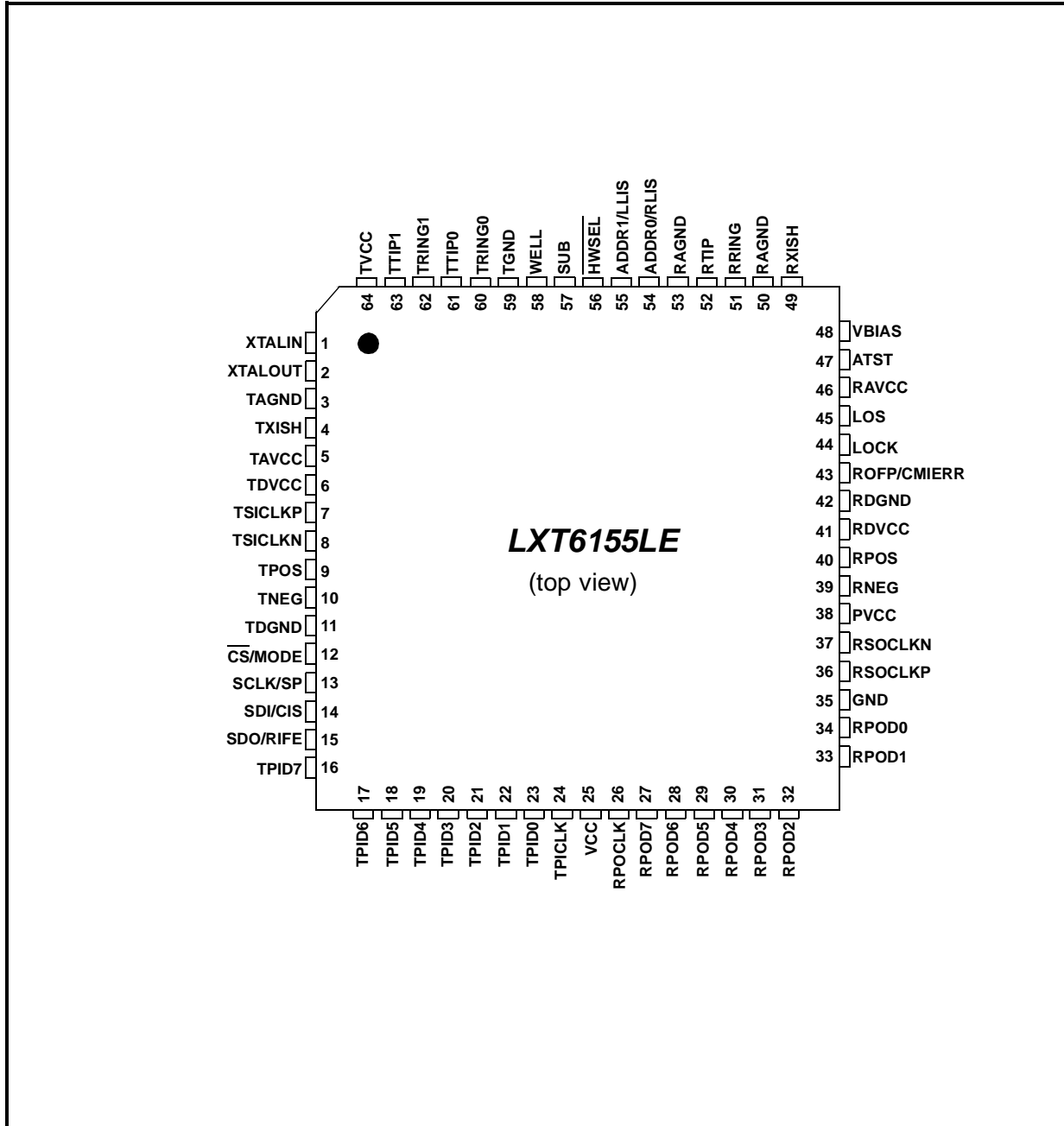
Table 1. LXT6155 Pin Descriptions

Pin #	Symbol	I/O[1]	Type[2]	Description
1	XTALIN	AI/O		**Crystal Input/Output**. These pins are connected to an external 19.44 MHz crystal. Alternately, a stable external clock signal may be connected to XTALIN with XTALOUT left open. XTALIN should be connected to TAGND and XTALOUT should be left open if the transmit input clock is used as a clock reference
2	XTALOUT			
3	TAGND	S		**Transmit Analog Ground.**
4	TXISH	AI/O		**Transmit PLL Loop Filter Pin.** Connecting a capacitor to TAGND from this pin controls the Tx PLL transfer function. This pin requires a 68nF cap to TAGND.
5	TAVCC	S		**Transmit Analog Power Supply.**
6	TDVCC	S		**Transmit Digital Power Supply.**
7	TSICLKP	DI	LVPECL	**Transmit Serial Input Clock, positive and negative**. Differential Transmit clocks at 155.52 MHz. These pins are disabled when parallel mode is selected.
8	TSICLKN			
9	TPOS	DI	LVPECL	**Transmit Serial Input Data, positive and negative.** Differential input data from an overhead terminator at 155.52 Mbps, clocked in by TSICLK. These pins are disabled when parallel mode is selected.
10	TNEG			
11	TDGND	S		**Transmit Digital Ground.**
12	CS/MODE	DI	TTL	**Chip Select Input, software mode** ($\overline{\text{HWSEL}}$ = High). Register transactions through the µP interface are initiated by the falling edge of this signal.
				Line Interface Mode, hardware mode ($\overline{\text{HWSEL}}$ = Low). Sets line interface mode to LVPECL (MODE = Low) or CMI (MODE = High).
13	SCLK/SP	DI	TTL	**Serial Clock Input, software mode** ($\overline{\text{HWSEL}}$ = High). Serial Microprocessor uses this pin to clock in/out data. SCLK can be from 0 to 4.096 MHz.
				Serial/Parallel Select, hardware mode ($\overline{\text{HWSEL}}$ = Low). When SP = Low, serial systems interface is used. When SP = High, 8 bit parallel system interface is used.
14	SDI/CIS	DI	TTL	**Serial Input Data, software mode** ($\overline{\text{HWSEL}}$ = High). The serial data is applied to this pin when the LXT6155 operates in software mode. SDI is sampled on the rising edge of SCLK.
				Clock Input Select, hardware mode ($\overline{\text{HWSEL}}$ = Low). CIS sets the reference clock for centering the Rx PLL. If CIS = Low, then the LXT6155 uses the transmit input clock as the reference. If CIS = High, then the LXT6155 uses the crystal clock input (XTALIN) as the reference.
15	SDO/RIFE	DI/O	TTL	**Serial Output Data, software mode** ($\overline{\text{HWSEL}}$ = High). The serial data from the on-chip register is output on this pin in software mode. Data output is valid on the rising edge of SCLK. This pin goes to a high impedance state when the serial port is being written to or when $\overline{\text{CS}}$ is High.
				Receive Input Frame Enabler, hardware mode ($\overline{\text{HWSEL}}$ = Low). The frame detection option is available only in parallel mode. If RIFE = Low, then the LXT6155 disables the frame detection, and byte alignment. If RIFE = High, then the LXT6155 enables the frame detection, and outputs RPOD bytes aligned to the SONET/SDH framer. This feature, if used, must be enabled prior to applying data to Rtip/Rring.

1. DI = Digital Input; DO = Digital Output; DI/O = Digital Input/Output; AI = Analog Input; AO = Analog Output; AI/O = Analog Input/Output; S=Supply.
2. TTL = Transistor-to-Transistor Logic (5V tolerant); LVPECL = Low-Voltage positive ECL.

Table 1.   LXT6155 Pin Descriptions (Continued)

Pin #	Symbol	I/O[1]	Type[2]	Description
16 17 18 19	TPID7/TXTRIM3 TPID6/TXTRIM2 TPID5/TXTRIM1 TPID4/TXTRIM0	DI	TTL	**Transmit Parallel Input Data**. Transmit data from an Overhead Terminator at parallel speed 19.44 MHz, clocked in by TPICLK. TPID7 is the most significant bit, and is the first bit to be sent. These pins should be grounded or not connected when the LXT6155 is used in serial mode.
				Transmit Trim Controls, in serial, hardware, coax mode only. These pins trim the amplitude of the line driver output from (nom -21%) to (nom +24%) in 3% steps. This feature is only enabled when pin #20 (TXTRIMENA) is High.
20	TPID3/TXTRIMENA	DI	TTL	**Transmit Parallel Input Data**. Transmit data from an Overhead Terminator at parallel speed 19.44 MHz, clocked in by TPICLK. TPID7 is the most significant bit, and is the first bit to be sent. These pins should be grounded or not connected when the LXT6155 is used in serial mode.
				Transmit Trim Enable, in serial, hardware, coax mode only. This pin enables the trimming of the line driver output by pins 16-19 when high.
21 22 23	TPID2 TPID1 TPID0	DI	TTL	**Transmit Parallel Input Data**. Transmit data from an Overhead Terminator at parallel speed 19.44 MHz, clocked in by TPICLK. TPID7 is the most significant bit, and is the first bit to be sent. These pins should be grounded or not connected when the LXT6155 is used in serial mode.
24	TPICLK	DI	TTL	**Transmit Parallel Input Clock**. Parallel transmit clock at 19.44 MHz. This pin is disabled when serial mode is selected and should be grounded or not connected.
25	VCC	S		**Power Supply**.
26	RPOCLK	DO	TTL	**Receive Parallel Output Clock**. Parallel receive clock as recovered from received data. The clock is nominally 19.44 MHz, synchronized with RPOD<7:0>.
27 28 29 30 31 32 33 34	RPOD7 RPOD6 RPOD5 RPOD4 RPOD3 RPOD2 RPOD1 RPOD0	DO	TTL	**Receive Parallel Output Data**. RPOD<7:0> output aligned 8-bit bytes at RPOCLK clock rate. These pins are to be left open when serial mode is selected. RPOD7 is the most significant bit, and is the first to arrive.
35	GND	S		**Ground**.
36	RSOCLKP	DO	LVPECL	**Receive Serial Output Clock**. Serial receive clock as recovered from received data. The clock is nominally 155.52 MHz, synchronized with output serial data RPOS and RNEG.
37	RSOCLKN			
38	PVCC	S		**PECL Buffers Power Supply**.
39	RNEG	DO	LVPECL	**Receive Serial Output Data, positive and negative**. These two pins provide recovered data synchronized to receive serial output clocks RSOCLKP and RSOCLKN. These pins are tristated and should be left open when parallel mode is selected.
40	RPOS			
41	RDVCC	S		**Receive Digital Power Supply**.
42	RDGND	S		**Receive Digital Ground**.

1. DI = Digital Input; DO = Digital Output; DI/O = Digital Input/Output; AI = Analog Input; AO = Analog Output; AI/O = Analog Input/Output; S=Supply.
2. TTL = Transistor-to-Transistor Logic (5V tolerant); LVPECL = Low-Voltage positive ECL.

Table 1. LXT6155 Pin Descriptions (Continued)

Pin #	Symbol	I/O[1]	Type[2]	Description
43	ROFP/ CMIERR	DO	TTL	**Receive Output Frame Pulse**. In hardware mode ($\overline{\text{HWSEL}}$ = Low), this pin is asserted (High) on the last A2 byte in the (A1.....A1, A2.....A2) sequence in the RPOD<7:0> traffic. A1=1111,0110 and A2=0010,1000 in binary. In software mode ($\overline{\text{HWSEL}}$ = High), this position is programmable. During coax operation, when frame detection is disabled (RIFE = 0 in HW/Reg #12, bit3 = 0), or in serial mode, this pin indicates CMI line code errors. These pulses are 50 ns wide (active high). One or more errors in 16 consecutive bits will causes a single pulse.
44	LOCK	DO	TTL	**Receive Output PLL Lock**. A High indicates receive PLL has locked to incoming data. A Low indicates receive PLL is not locked.
45	LOS	DO	TTL	**Loss of Signal**. An alarm output signal (high) indicating incoming signal voltage is weak or incoming data does not contain enough transitions. In software mode ($\overline{\text{HWSEL}}$ = 1) this pin can be configured to combine LOS and LOCK alarms.
46	RAVCC	S		**Receive Analog Power Supply**.
47	ATST	-		**Analog Test**. For factory test purposes only; do not connect.
48	VBIAS	AI	Analog	**Bias Input Voltage.** This pin requires a 15K (1%) pull-down resistor to RAGND.
49	RXISH	A0	Analog	**Rx PLL External Cap.** Connecting a capacitor to RAGND from this pin controls the Rx PLL transfer function. This pin requires a 330nF cap to RAGND.
50	RAGND	S		**Receive Analog Ground**.
51	RRING	AI	Analog	**Receive Input Data, positive (RTIP) and negative (RRING)**. Accepts incoming signals (LVPECL or CMI) from the line interface.
52	RTIP			
53	RAGND	S		**Receive Analog Ground**.
54	ADDR0/RLIS	DI	TTL	**Address 0, software mode** ($\overline{\text{HWSEL}}$ = High). This pin together with ADDR1 sets the chip select address. Up to 4 LXT6155 chips can be addressed by the μP interface. **Remote Loopback Input Select, hardware mode** ($\overline{\text{HWSEL}}$ = Low). Together with LLIS sets LXT6155 in a loopback test mode. See Table 4
55	ADDR1/LLIS	DI	TTL	**Address 1, software mode** ($\overline{\text{HWSEL}}$ = High). This pin together with ADDR0 sets the chip select address. Up to 4 LXT6155 chips can be addressed by the μP interface. **Local Loopback Input Select, hardware mode** ($\overline{\text{HWSEL}}$ = Low). Together with RLIS sets the LXT6155 in remote loopback mode. See Table 4
56	HWSEL	DI	TTL	**Hardware/Software Mode Select**. When $\overline{\text{HWSEL}}$ = High, LXT6155 enters software (host) mode, and is ready to communicate with a serial microprocessor. When $\overline{\text{HWSEL}}$ = Low, LXT6155 operates in hardware standalone mode (without a serial μP).
57	SUB	S		**Reserved**. Must be connected to GND.
58	WELL	S		**Reserved**. Must be connected to VCC.
59	TGND	S		**Transmit Analog Ground**.
60	TRING0	AO		**Transmit Output Data, positive (TTIP0) and negative (TRING0)**. Differential CMI driver outputs for coax interface.
61	TTIP0			

1. DI = Digital Input; DO = Digital Output; DI/O = Digital Input/Output; AI = Analog Input; AO = Analog Output; AI/O = Analog Input/Output; S=Supply.
2. TTL = Transistor-to-Transistor Logic (5V tolerant); LVPECL = Low-Voltage positive ECL.

Table 1.   LXT6155 Pin Descriptions (Continued)

Pin #	Symbol	I/O[1]	Type[2]	Description
62	TRING1	DO		**Transmit Output Data, positive (TTIP1) and negative (TRING1).** Differential LVPECL NRZ driver outputs for a fiber optic transceiver.
63	TTIP1			
64	TVCC	S		**Transmit Analog Power Supply**.
1. DI = Digital Input; DO = Digital Output; DI/O = Digital Input/Output; AI = Analog Input; AO = Analog Output; AI/O = Analog Input/Output; S=Supply. 2. TTL = Transistor-to-Transistor Logic (5V tolerant); LVPECL = Low-Voltage positive ECL.				

2.0 Functional Description

The LXT6155 is a front-end transceiver designed for 155 Mbps OC3/STM1/ATM transmission applications. Table 2 lists the standards with which the LXT6155 is compliant.

The LXT6155 interfaces to either a fiber transceiver or a coax cable on the line side, and on the system side, to an SDH/SONET Overhead Terminator or an ATM UNI. The LXT6155 can function in Hardware stand-alone mode, or in Software mode controlled through an industry standard Motorola compatible 4-wire serial microprocessor interface.

The LXT6155 can be set to operate in either CMI mode for the 75Ω coax interface or NRZ mode for the optical transceiver interface. The operating mode can be set in either hardware mode by using the MODE pin, or software mode by using Primary Control Register, bit 0.

2.1 Transmitter

In serial mode, the LXT6155 accepts both data (TPOS, TNEG) and clock signals (TSICLKP, TSICLKN). Serial clock signals are required for the LXT6155 to run internal logic, reshape the line transmit pulses and generate the low-jitter clocks for Tx data generation.

In parallel mode, the LXT6155 accepts data TPID<7:0> and clock TPICLK. TPICLK is internally multiplied by 8 to yield the 155.52 MHz clock for Tx data generation.

Both serial and parallel clocks (TSICLKP/TSICLKN and TPICLK) must conform to the SONET/SDH standard frequency accuracy requirements.

Depending on whether the selected media interface is coax or fiber, the data is CMI or NRZ encoded respectively, and passed to the appropriate line drivers. The LXT6155 line drivers are high-speed buffers that meet the CMI templates and industry standard LVPECL signal requirements. The CMI output pins are TTIP0 and TRING0, and the NRZ LVPECL pins, TTIP1 and TRING1.

2.1.1 Transmitted Signal

Transmitted signals conform to the standard templates listed in Table 2.

2.1.1.1 Fiber Based G.957/GR-253 Transmission Systems

The LXT6155 provides 3.3V LVPECL compatible signals for interfacing to a fiber optic transceiver. Please refer to Application Information for interface schematics.

2.1.2 Coax Based G.703/GR-253 Transmission Systems

The LXT6155 encodes and decodes CMI signals that are transmitted onto a 75 Ω coax cable compliant with STM1/STS-3 CMI templates. Please refer to the CMI templates shown in Figures 24 and 25.

Figure 2. LXT6155 System Interface
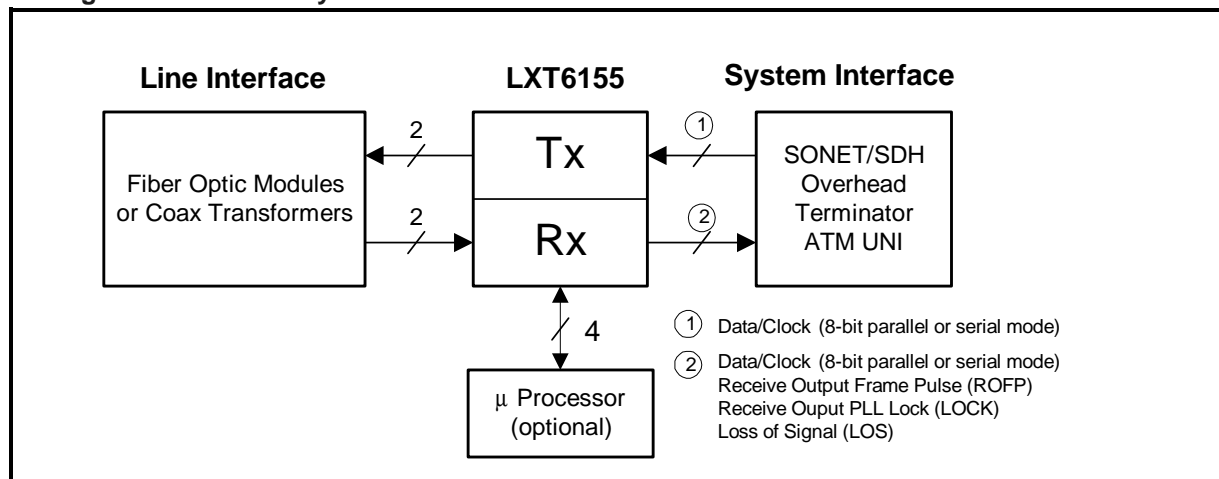
2.1.2.1 CMI Encoding

Coded Mark Inversion (CMI) is an encoding scheme adopted by SONET STS-3 and SDH STM1 standards. CMI encoding guarantees at least one transition per bit, thereby enhancing the clock recovery process. CMI encodes a "0" with a midpoint positive transition, and a "1" as Low or High, in opposite polarity to the previous encoded "1". Refer to Figures 6, 24 and 25 for encoding and pulse template information.

2.1.3 Tx Clock Monitoring

The LXT6155 provides transmit clock monitoring for both serial and parallel operating modes. When using the crystal clock as a reference, the LXT6155 monitors the TSICLKP/TSICLKN or the TPICLK input(s) for transitions. If no transition is seen within 200ns, the tx_clk_alarm flag will be set (reg #15) and the transmitter outputs ttip1/tring1 or ttip0/tring0 will stop sending data to the line. This condition will remain until the LXT6155 detects clock transitions at the transmitter input(s) TSICLKP/TSICLKN or TPICLK. Transmit clock monitoring can be disabled in software mode only.

In remote loopback, transmit clock monitoring is disabled in SW and HW mode. In SW mode, when using transmit clocks as the receive PLL reference, the user must disable transmit clock monitoring by setting reg #1 bit <0> low.

2.2 Receiver

2.2.1 Analog Front End and Timing Recovery

2.2.1.1 CMI Mode

Received data on RTIP/RRING goes through an adaptive equalizer. An adaptive $\sqrt{f}$ equalizer and adaptive Automatic Gain Control (AGC) compensate the frequency-and-cable length dependent loss in data signal, and reshapes the signal to the optimal waveform. A Phase Locked Loop (PLL)

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then performs clock recovery operation, comparing the reshaped data phase against the receive output clock phase. The receive PLL requires an external reference (e.g. transmit input clock or XTAL clock) to start up the clock recovery process. This clock can be derived from XTALIN, TPICLK or TSICLK (÷8). The recovered clock is used to retime the CMI signals, and to decode CMI to NRZ. Coding errors are detected and flagged via the CMIERR pin in HW mode with the frame detect disabled or in serial mode. In software mode ($\overline{\text{HWSEL}}$ = High) CMI coding errors are indicated via the µP interface interrupt register: Reg #15, mode 05.

2.2.1.2 NRZ Mode

The on chip adaptive equalizer is bypassed. Data goes straight to the clock recovery phase locked loop. The PLL then performs clock recovery operation, comparing the data phase against the clock phase. This clock can be derived from XTALIN, TPICLK or TSICLK (÷8). The receive PLL requires an external reference (e.g. transmit input clock or XTAL clock) to start up the clock recovery process.

The recovered clock is used to retime the data signals. When the recovered clock is within 488 ppm of the reference clock, the LOCK signal asserts. This alarm is also accessible on the µP interface as a status bit (Reg #15, mode 0) and as an interrupt (Reg #15, mode 05). Once the recovered clock has been obtained and the NRZ data has been recovered, the LXT6155 performs frame-detect-and-byte-alignment, and serial-to-parallel conversion. The LXT6155 optionally provides output data RPOD<7:0> aligned to the SDH/SONET byte boundary. The user has the option to enable/disable the frame-alignment function in both hardware and software mode. The frame detect/byte alignment function generates the receive output frame pulse (ROFP). In HW mode ($\overline{\text{HWSEL}}$ = Low) ROFP asserts (high) on the third A2 byte. In SW mode ($\overline{\text{HWSEL}}$ = High) this position is programmable via register #13, bits <6:3>. When byte alignment is disabled and the LXT6155 is in CMI mode, the ROFP pin indicates CMI coding errors including polarity errors for ones and inversion errors for zeroes.

The clock recovery PLL's center frequency comes from either the local crystal or a stable transmit input clock (TSICLKP/TSICLKN or TPICLK). If operated in loop-timed mode or remote loopback mode, an external reference clock must be used to center the internal PLL clock. In remote loopback, the receive reference remains either XTALIN or TSICLK or TPICLK, depending on the control selection. If an independent and stable transmit clock is available, the designer has the option of applying this clock to pin XTALIN to center the PLL, without the external crystal.

The user can also replace the crystal by connecting the TPICLK (19.44MHz) signal to the XTALIN pin. However, a local crystal is recommended for "keep alive" purposes in case the clock becomes unavailable.

2.2.2 Receive Frame Detect and Byte Alignment

Receive Frame Detection only operates in parallel mode, if Frame Detection is enabled. The LXT6155 provides aligned bytes RPOD<7:0> following the distinct SONET OC3/STM1 frame marker word, 3 x A1, followed by 3 x A2, where A1=F6h and A2=28h. The Receive Output Frame Pulse (ROFP) asserts during the third A2 byte, and de-asserts after one complete RPOCLK clock period. If this feature is used, it can be enabled in register #12 bit <3> in software mode[1], or by setting the RIFE (pin 15) high in hardware mode prior to applying data to Rtip/Rring. Two consecutive frames with correct frame words ($A_1...A_1\ A_2...A_2$) are required to change from an out-of-frame state (OOF) to an in-frame state. The OOF alarm is accessible in SW mode ($\overline{\text{HWSEL}}$ = High) as a status or interrupt signal (Reg #15). To declare an OOF condition, four consecutive

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1. For further details see register #12 description for usage.

frames with incorrect frame words are required. Byte alignment occurs when entering the in-frame state. In case of an OOF event, the byte alignment and frame pulse position are frozen. The ROFP output continues unchanged until re-entering the in-frame state.

Figure 3. Framing State
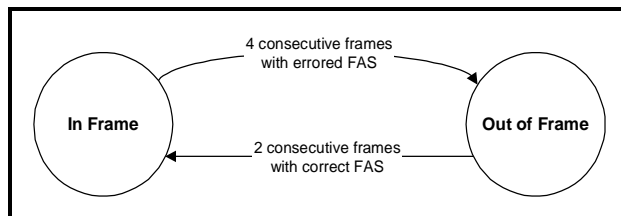
2.2.2.1 Loss of Signal (LOS)

Loss of Signal provides an alarm signal indicating incoming signal voltage is weak or incoming data does not contain enough transitions. This signal is available in HW mode on pin #45 and in SW mode as status and interrupt (Reg #15, modes 00 and 05).

2.2.2.2 Coax Interface

Loss of Signal provides an alarm output that indicates weak line input signal. The LOS signal asserts when the incoming signals fall below a specified loss threshold, and de-asserts when the line signal rises nominally 2dB above the assert threshold. The threshold is adjustable in SW mode ($\overline{HWSEL}$ = High) via the µProcessor interface.

2.2.2.3 Fiber Interface

If no transition is detected during any 3112 bit times (20 µsec), LOS asserts. LOS is cleared when two consecutive frame words with no LOS events between then are received. In SW mode ($\overline{HWSEL}$ = High) the assertion window is programmable from 128 bits to 4096 bits in four steps. The deassertion criteria can also be configured to 12.5% transition density. The 12.5% density is determined by receipt of at least 4 transitions during a 32 bit sliding window.

Figure 4. Criteria for LOS Output
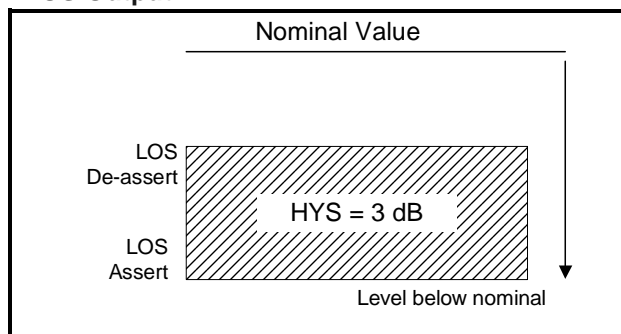
Figure 5. Receive Frame Synchronization and Frame Pulse Position
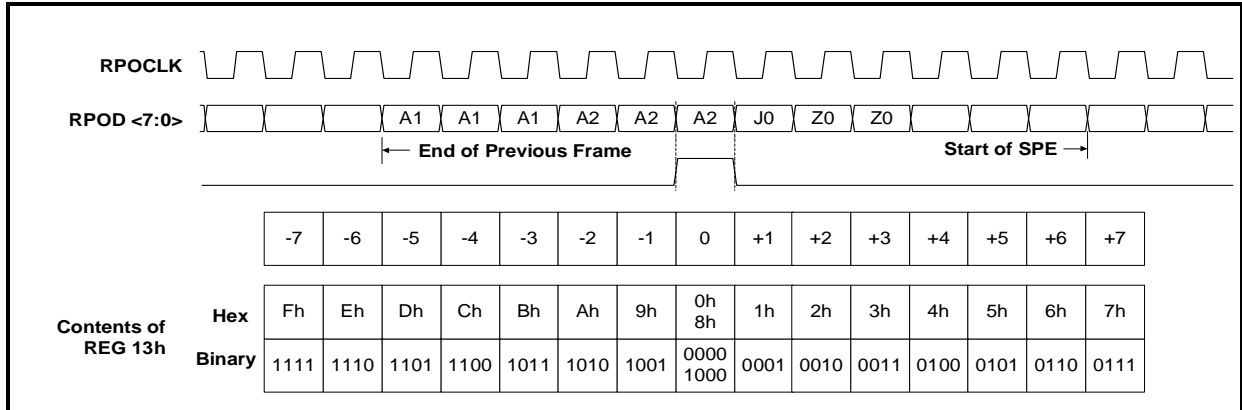
Table 2. Standards Compliance

Item	SDH/SONET (Fiber)		SDH/SONET (Coax)	
	STM1	**OC3**	**STM1**	**STS-3**
Line Rate (Mbps)	155	155	155	155
Line Interface	50 Ω LVPECL	50 Ω LVPECL	75 Ω coax	75 Ω coax
Line Code	NRZ	NRZ	CMI	CMI
Signal Templates	G.957 STM1 Eye	OC3 OC3 Eye	G.703 CMI Template. CMI Eye	STSX-3 CMI Template. CMI Eye
Jitter	G.958 G.825	GR-253	G.813 G.825	GR-253

Figure 6. Example of CMI Encoded Binary Signal
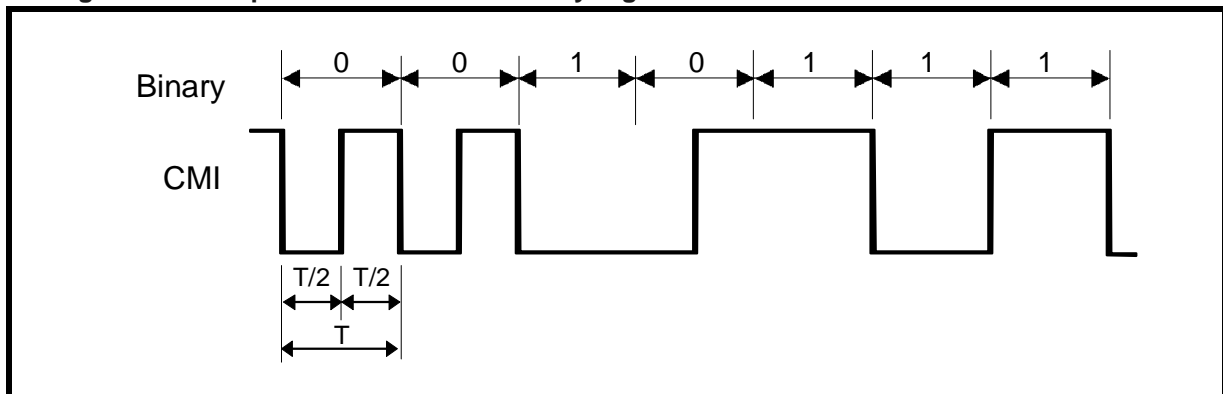
2.3 Clocks

2.3.1 Parallel Mode

The LXT6155 accepts TPICLK synchronized with transmit input parallel data TPID<7:0>. The data is serialized and transmitted at TTIP0/TRING0 or TTIP1/TRING1 depending on which line encoding mode is selected. The LXT6155 in turn produces the receive output parallel clock RPOCLK, that is recovered from incoming line data RTIP/RRING, and is synchronized with receive output parallel data RPOD<7:0>.

2.3.1.1 Transmit Parallel Input Clock (TPICLK)

TPICLK is the transmit parallel input clock provided by the systems interface. This clock must be nominally 19.44 MHz, synchronized with parallel input data TPID<7:0>. This clock is then internally multiplied by 8 to produce a serial clock, used for parallel-to-serial conversion, line drivers, and pulse reshaping. In HW mode ($\overline{\text{HWSEL}}$ = Low), TPID data is sampled on the falling edge of TPICLK. In SW mode ($\overline{\text{HWSEL}}$ = High), the clock polarity can be inverted (Reg #0, bit #3).

2.3.1.2 Receive Parallel Output Clock (RPOCLK)

RPOCLK is the parallel output clock that is recovered from the line input data RTIP/RRING. This clock is at 19.44 MHz, synchronized with parallel output data RP0D<7:0>. In HW mode ($\overline{\text{HWSEL}}$ = Low), the RPOCLK clock rising edge is at the center of eye opening of RPOD<7:0> as shown in Figure 21. In SW mode ($\overline{\text{HWSEL}}$ = High), the clock polarity can be inverted (Reg #0, bit #2). Under LOS (LOS=High) or Rx PLL loss of lock (LOCK=Low) conditions RPOCLK is switched to the reference selected by the CIS control in HW mode, or Reg #0 bit #5 in SW mode. Also, the parallel output is forced to all zeros. This feature can be disabled in SW mode ($\overline{\text{HWSEL}}$ = High) via register #10, bit #7.

2.3.2 Serial Mode

At the transmit systems interface, the LXT6155 accepts the transmit input clock TSICLKP/TSICLKN that is synchronized to incoming serial differential data TPOS/TNEG. At the line interface, the LXT6155 accepts RTIP/RRING data and produces the clocks RSOCLKP/RSOCLKN synchronized to receive output data RPOS/RNEG. RSOCLKP/RSOCLKN clock edges are at the center of RPOS/RNEG.

2.3.2.1 Transmit Serial Input Clock (TSICLKP/TSICLKN)

TSICLKP/TSICLKN is the serial input clock from the overhead terminator. This 155.52 MHz clock is rising edge centered with input serial data on TPOS and TNEG. These clock pins should be left open when the LXT6155 operates in parallel mode.

2.3.2.2 Receive Serial Output Clock (RSOCLKP/RSOCLKN)

RSOCLKP/RSOCLKN is the serial clock recovered from the line input data on RTIP/RRING. This 155.52 MHz clock is falling edge centered with receive serial output data on RPOS/RNEG. These clock pins should be left open when the LXT6155 operates in parallel mode. Under LOS

(LOS=High) or Rx PLL loss of lock (LOCK=Low) conditions RSOCLK P/N is switched to the Tx serial clock. Also the serial output data is forced to all zeros. This feature can be disabled in SW mode ($\overline{\text{HWSEL}}$ = High) via register #10, bit #7.

2.3.3 Crystal Reference Clock (XTALIN/XTALOUT)

An optional 19.44 MHz crystal can be connected across the XTALIN and XTALOUT pins. This crystal reference provides an onchip clock that is independent of the external system clock (TSICLKP/TSICLKN or TPICLK). The main functions of the crystal reference clock are threefold: (1) to center the receive PLL at 155 MHz, (2) to keep the PLL centered at 155 MHz when LOS asserts, and (3) In the event incoming data is lost, to provide a reference clock for other devices which require it. The designer has the option to use this crystal reference clock or the transmit input clock (TSICLKP/TSICLKN or TPICLK) to center the receive PLL.

2.4 Jitter

The Bellcore GR-253 standard defines jitter as the "short-term variations of a digital signal's significant instants from their ideal positions in time". Significant instants are the optimum data sampling instants. Jitter parameters can be measured at the line interface, with system interface in loopback mode, yielding jitter accumulated in both transmitter and receiver. Isolated jitter measurements for transmitter and receiver can also be performed. Jitter specs are divided into three categories: jitter tolerance, jitter generation, and jitter transfer. Jitter values, in effect, measure the performance of the receive PLL and the transmit synthesizer PLL.

2.4.1 Jitter Tolerance

Jitter tolerance is the peak-to-peak amplitude of sinusoidal jitter applied at the line interface input that causes an equivalent 1 dB SNR loss measured as BER = 10^{-10}. Refer to Figure 26 on page page 44 for the LXT6155 performance.

2.4.2 Jitter Generation (Intrinsic Jitter)

Jitter generation is the amount of transmit jitter at the output of the equipment with a jitter-free transmit input data and clock. For SONET/SDH, jitter generation is less than 0.01 UI rms, measured with a band-pass filter from 12 kHz to 1.3 MHz. Refer to 27 on page 45 for the LXT6155 performance.

2.4.3 Jitter Transfer

Jitter transfer is defined as the ratio of output jitter to input jitter amplitude versus jitter frequency for a given bit rate. Input jitter amplitude is shown in the Jitter Tolerance curve. Output jitter is under the Jitter Transfer template. Refer to Figures 27 and 28 on pages and for the LXT6155 performance.

2.5 Operational Modes

The LXT6155 functions in both Hardware standalone and Software modes. The operating mode is set by the state of the $\overline{\text{HWSEL}}$ pin.

2.5.1   Hardware Mode

By setting $\overline{\text{HWSEL}}$ = Low, the LXT6155 operates in standalone hardware mode, without a serial microprocessor interface. A subset of the functions available in the Software Mode can be set in Hardware Mode. LXT6155 provides a comprehensive flexibility in configuring system clock preference settings, as well as providing pins for activating loopback test modes. Tables 3, 4 and 5 show the settings that enable the functions available in hardware mode.
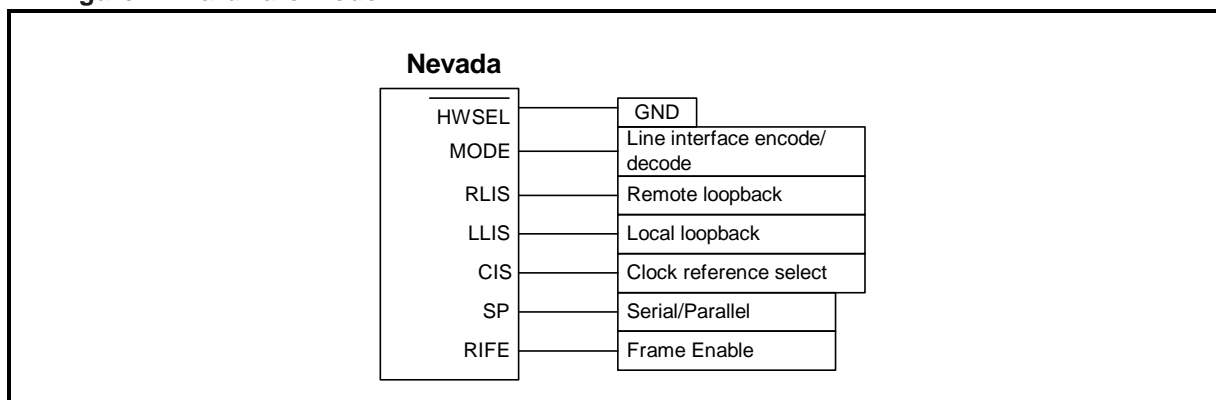
Figure 7. Hardware Mode

Table 3.   Reference Clock Settings[1]

CIS	Clock Reference	Note
Low	TICLK	Default mode. The LXT6155 uses the transmit input clock as the reference clock for on chip operations. No crystal is needed.
High	XTAL	The LXT6155 uses the clock signal at XTALIN as the reference clock for Rx operation. This can either be an applied 19.44MHz clock or a 19.44MHz crystal can be connected across XTALIN & XTALOUT. See Table 24 for the crystal specifications.
1. For explanation, see clock sections below.		

2.5.1.1   PLL Clock Reference (CIS pin)

The reference clock plays two roles: it centers the receive PLL, and it provides the receive output clocks RSOCLKP/RSOCKLN and RPOCLK in case of Loss of Signal. When the LXT6155 powers up, it looks for this reference clock to start-up internal blocks, including the receive PLL circuitry.

2.5.1.1.1   TICLK

This is the transmit input clock(s): either TSICLKP/TSICLKN in serial mode or TPICLK in parallel mode.

2.5.1.1.2   XTAL

XTAL is an optional clock, created using an external crystal, connected across the XTALIN and XTALOUT pins. The crystal provides an independent and stable clock source. This clock is also used as the reference for the Tx clock monitoring circuitry.

2.5.1.2   Loopback Test (RLIS and LLIS pins)

The LXT6155 allows two types of loopback test: Remote loopback and Local loopback. In Remote loopback, the received data and clock are looped back to the transmit line interface. The LXT6155 still outputs recovered data and clock at the system interface. In Local loopback, the transmit data is looped back to the receive input at the line interface. The LXT6155 also transmit data onto the line interface while looping back. For descriptive diagrams, please refer to Figures 13 and 14.

Table 4.   Loopback Selection

RLIS	LLIS	Description
Low	Low	Normal operation. No loopback testing.
Low	High	Local loopback test activate.
High	Low	Remote loopback test activate.
High	High	

2.5.1.3   Line Interface Selection (MODE Pin)

The MODE pin sets one of the two line interfaces, as described in Table 5.

Table 5.   MODE Line Interface Settings

MODE	Description
Low	Sets LVPECL NRZ mode to interface to a fiber optic module. CMI related blocks (e.g. input/output buffers, equalizer) are disabled.
High	Sets CMI mode to interface to a transformer and a 75Ω coax cable. NRZ related input/output buffers are disabled.

2.5.1.4   Parallel/Serial Mode Selection (SP pin)

In Hardware Mode, $\overline{\text{HWSEL}}$ = Low, the LXT6155 can be set to operate in serial or parallel data mode, depending on how the Serial/Parallel SP pin is set.

Setting the SP pin = High sets the LXT6155 to an 8-bit parallel mode. Parallel pins TPID<7:0>, TPICLK, RPOD<7:0>, ROFP, RPOCLK, LOCK and LOS are be used. Serial pins TPOS, TNEG, TSICLKP, TSICLKN, RPOS, RNEG, RSOCLKP, RSOCLKN are unused and should be left open.

Setting the SP pin = Low sets the LXT6155 to serial mode. Pins TPOS, TNEG, TSICLKP, TSICLKN, RPOS, RNEG, RSOCLKP, RSOCLKN, LOCK and LOS are used. Pins TPID<7:0>, TPICLK, RPOD<7:0> and RPOCLK are unused and should be left open.

2.5.1.5   Tx Amplitude Trim

In Hardware, serial, coax mode, the line driver output amplitude can be controlled via pins 16 to 20. Setting TXTRIMENA (pin #20) high enables the trim capability. The trim rage is -21% to +24% in 3% steps controlled by TXTRIM0-TXTRIM3. The minimum amplitude is at 0000 and the maximum amplitude is at 1111. This is the same control range as in SW mode.

2.5.2 Software Mode

When $\overline{\text{HWSEL}}$ = High, the LXT6155 operates in Software Mode. Control is through an external serial µP interface. Figure 8 shows the pins used in Software Mode. The LXT6155 uses four pins for the industry standard Serial Control Interface (SCP) bus: SCLK, $\overline{\text{CS}}$, SDI and SDO. SCLK is the serial input control clock pin. $\overline{\text{CS}}$ is the chip select input. SDI is the serial data input pin, and SDO is the serial data output pin. Figures 9 and 10 show the serial interface data structure. A data transaction is initiated by a falling edge on the Chip Select pin $\overline{\text{CS}}$. A High-to-Low transition on $\overline{\text{CS}}$ is required for each access to the control registers. The first bit is a read/write bit (R/$\overline{\text{W}}$), followed by seven address bits (A<6:0>), and eight data bits (D<7:0>). Every data transaction requires 16 SCLK cycles to complete. If R/$\overline{\text{W}}$ = High (Read), the LXT6155 outputs a data byte D<7:0> on the SDO pin. If R/$\overline{\text{W}}$ = Low (Write), the LXT6155 accepts a data byte D<7:0> on the SDI pin, while tristating SDO pin.

It is recommended in SW mode operation, the registers are first initialized by writing a "0" to register #11 bit #6 (reset).

2.5.2.1 Serial Input Clock (SCLK)

This pin accepts a clock up to 4.096 MHz for data transactions between the LXT6155 and the SCP bus. The LXT6155 clocks SDO data out on the falling edge, and clocks SDI data in on the rising edge of SCLK (see Figures 9 and 10).

2.5.2.2 Chip Select Input ($\overline{\text{CS}}$)

On the falling edge of $\overline{\text{CS}}$, the LXT6155 starts data transactions. On the rising edge of $\overline{\text{CS}}$, the LXT6155 stops data transaction. The $\overline{\text{CS}}$ pin must be held Low for at least 16 SCLK cycles to complete a full Read or Write data transaction. If $\overline{\text{CS}}$ is held Low less than 16 SCLK cycles, then the data transaction is ignored. At the end of each Write/Read transaction, $\overline{\text{CS}}$ must return High, between the 16th and 17th clock edges.

2.5.2.3 Serial Input Word (SDI)

Figure 10 shows the serial interface input data word structure. When the first input bit R/$\overline{\text{W}}$ = Low, a Write operation is performed. The SCLK clocks data in on the SDI pin during the second 8 bits D<7:0> of the Write operation. Data is clocked in on the rising edge of SCLK. During the entire 16 bit operation, SDO remains tristated. Refer to Tables 6 through 22 for control register descriptions.

2.5.2.4 Serial Output Word (SDO)

The serial output word structure is shown in Figure 9. When the first input bit R/$\overline{\text{W}}$ = High, a Read operation is specified. SDO becomes active after A0 has been clocked in. The first bit out of SDO changes the state of SDO from High-Z to a Low/High. SDO is clocked out on the falling edge of SCLK.

Figure 8. Software Mode
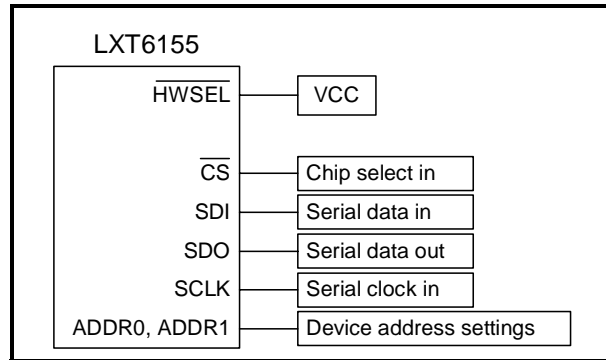
Figure 9. Serial Data Output Word Structure (Read Cycle: R/W̄=High)
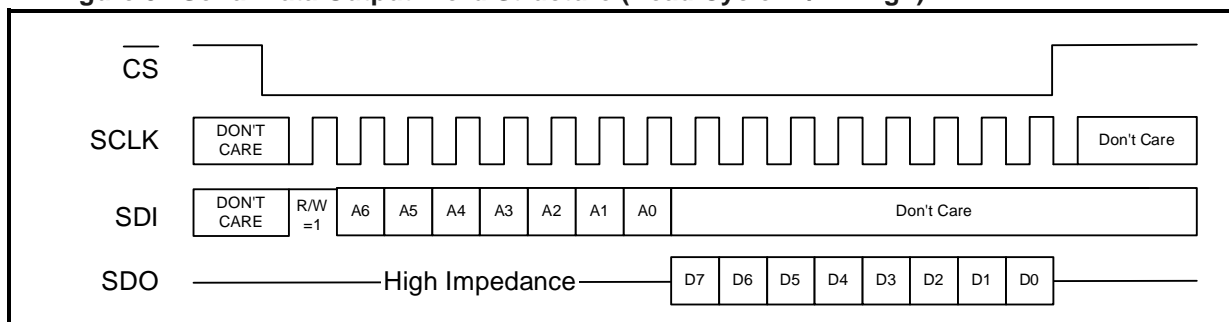
Figure 10. Serial Data Input Word Structure (Write Cycle: R/W̄ = Low)
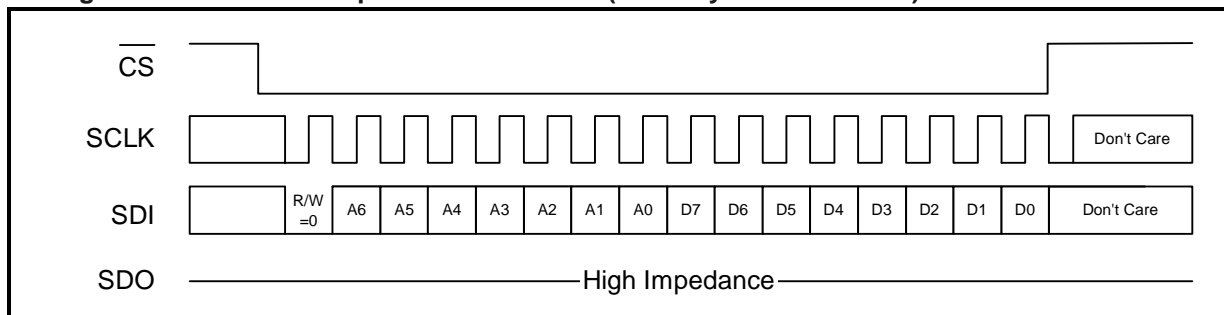
2.6 Serial System Interface

The serial interface permits the LXT6155 to communicate with an Overhead Termination device at 155.52 Mbps. Data and clock lines are differential 3.3V LVPECL signals. Refer to Figure 11.

2.7 Parallel System Interface

Parallel interface allows the LXT6155 to communicate with the system chip at 19.44 MHz, 8 bits per clock cycle. Data and clock lines are TTL compatible signals. Refer to Figure 12.

Figure 11. Serial Interface
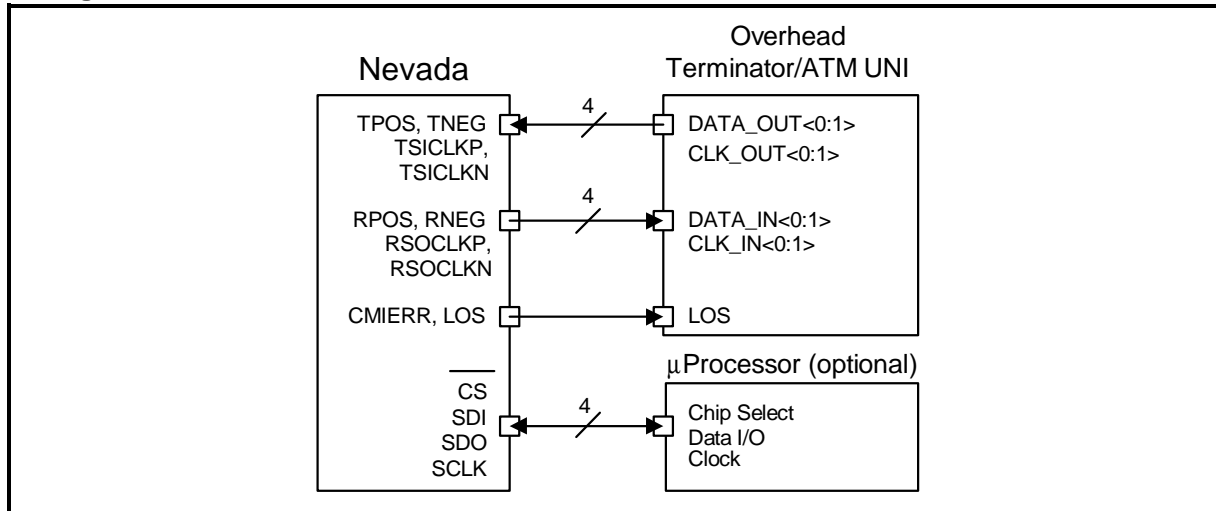
Figure 12. Parallel Interface
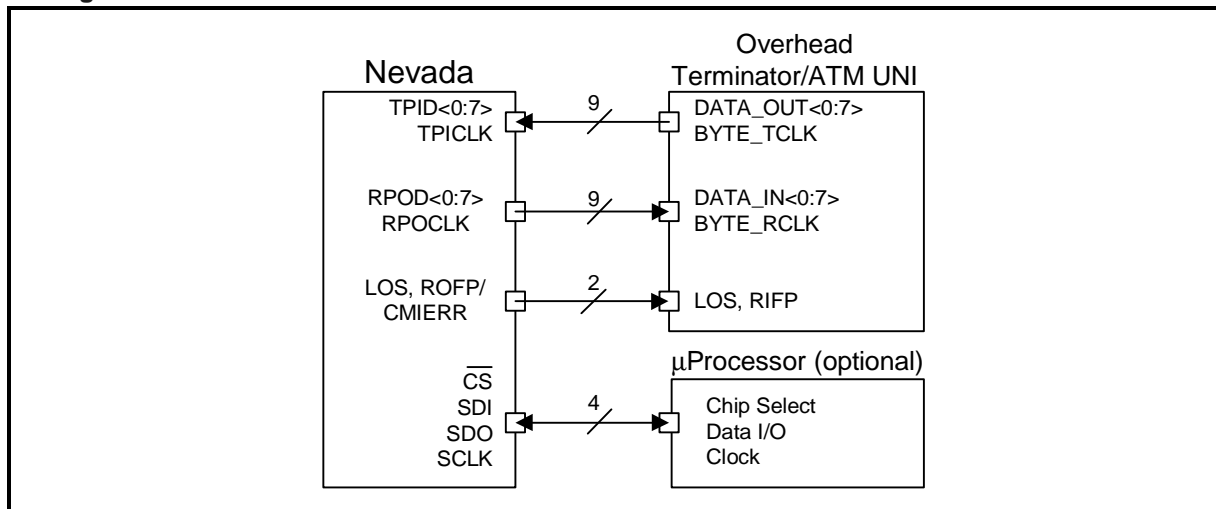
2.8 Loopback Modes

The LXT6155 provides two loopback modes that can be executed in either hardware or software mode: local loopback and remote loopback. In remote loopback mode, the crystal reference clock is used to center the receive PLL to prevent illegal clock looping.

2.8.1 Local Loopback

Local loopback routes the transmit line output signals (TTIP and TRING) back to the receive line inputs (RTIP and RRING). In this mode, the line transmit output signals are active (see Figure 13).

2.8.2 Remote Loopback

Remote loopback routes the receive system output signals, both data and clock, to the transmit system input (see Figure 14). In this mode, system outputs (RPOD<7:0> or RPOS/RNEG) are still active.

Figure 13. Local Loopback
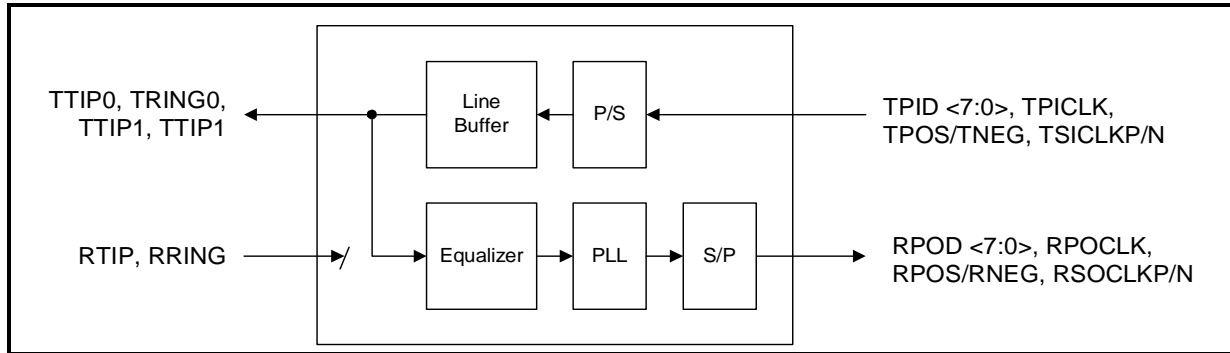
Figure 14. Remote Loopback
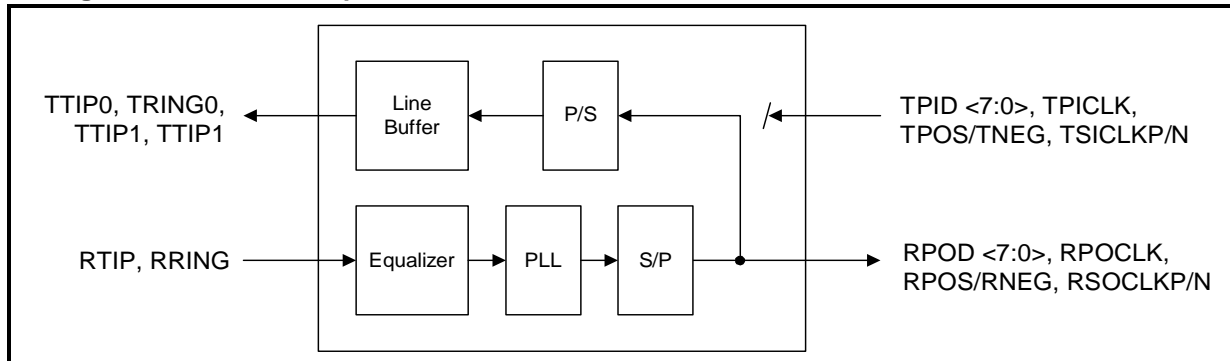
3.0   Register Definitions

There are a total of sixteen (16) control registers in the LXT6155 addressed by the lowest four address bits, A<3:0>. See Tables 8 through 22 for details .

Table 6.   Device Address/Control Byte

A<6:0>	Description
A<6:5>	LXT6155 Device Select. By using pins ADDR1 and ADDR0, up to four LXT6155 devices can be addressed. For a successful data transaction to occur, A6 and A5 must match the polarity settings on ADDR1 and ADDR0, respectively. Using these controls, up to four LXT6155 devices can be independently controlled.
A4	Not Used. Set to 0 during transactions.
A<3:0>	LXT6155 Register Map (see Table 7).

Table 7.   LXT6155 Register Map (A<3:0>)

Register #	A<3:0>	Register Name	Type
0	0000	Primary Control	R/W
1	0001	Transmit Control	R/W
2	0010	Transmit PLL1	R/W
3	0011	Transmit PLL2	R/W
4	0100	Equalizer load	R/W
5	0101	Equalizer/AGC	R/W
6	0110	Matching filter2	R/W
7	0111	Slicer	R/W
8	1000	Receive PLL 1	R/W
9	1001	Receive PLL 2	R/W
10	1010	Test	R/W
11	1011	Reset and Bias	R/W
12	1100	Receive Digital 1	R/W
13	1101	Receive Digital 2	R/W
14	1110	Status/Interrupt Control	R/W
15	1111	Status/Interrupt Output	Read-only

Table 8.   Primary Control Register Settings, Register #0 (Address A<3:0>=0000)

Bit	Default	Mnemonic	Description
7	0	lpbk_cntl	Local loopback: 0 = No loopback 1 = Activate local loopback
6	0		Remote loopback: 0 = No loopback 1 = Activate remote loopback
5	0	pll_ref	PLL/Equalizer reference clock control: 0 = Use TPICLK clock 1 = Use external crystal (XTALIN)
4	0	-	Not used
3	1	clk_inv	T$_{PICLK}$ polarity at system interface: 0 = TPID <7:0> sampled on the rising edge of TPICLK 1 = TPID <7:0> sampled on the falling edge of TPICLK
2	1		R$_{POCLK}$ polarity at system interface: 0 = RPOD <7:0> transitions on the rising edge of RPOCLK 1 = RPOD <7:0> transitions on the falling edge of RPOCLK
1	0	sys_int	Systems interface mode selection: 0 = Serial mode 1 = Parallel 8 bit mode
0	0	media_sel	Media and line code selection: 0 = Fiber (NRZ) 1 = Coax (CMI)

.

Table 9.   Tx Control, Register #1 (Address A<3:0>=0001)

Bit	Default	Mnemonic	Description
7	1	tx_ena	Tx output enable: 0 = outputs disabled 1 = outputs active
6	1	tx_dig_reset	Tx digital circuitry reset. This can be used to minimize power comsumption when the device is disabled but not powered down. It must be enabled when the device is active. 0 = reset 1 = active
5	0		
4:1	0.1.1.1	tx_amp_trim	Transmit amplitude trim: 0000 = -21% 1111 = +24%
0	1	tx_clk_sw_ena	Tx clock detection enable. This must be disabled in SW mode when pll_ref=0 (reg#0<5>=0) 0 = disable 1 = enable

Table 10. Transmit PLL1, Register #2 (Address A<3:0>=0010)

Bit	Default	Mnemonic	Description
7:5	0.1.1		Not for customer use
4:3	0.0		Not for customer use
2:1	1.0		Not for customer use
0	1		Not for customer use

Table 11. Transmit PLL2, Register #3 (Address A<3:0>=0011)

Bit	Default	Mnemonic	Description
7	1		Not for customer use
6	1		Not for customer use
5	1		Not for customer use
4	0		Not for customer use
3	0		Not for customer use
2	0		Not for customer use
1:0	1.0		Not for customer use

Table 12. Equalizer Load, Register #4 (Address A<3:0>=0100)

Bit	Default	Mnemonic	Description
7	0		Not for customer use
6:2	0.0.0.0.0		Not for customer use
1	0		Not for customer use
0	1		Not for customer use

Table 13. Equalizer & AGC, Register #5 (Address A<3:0>=0101)

Bit	Default	Mnemonic	Description
7	1	eq_adapt_enab	Equalizer adaption enable: 0 = freeze adaption 1 = activate adaption
6:5	0.0	eq_adapt_gain	Equalizer adaption step size: 00 = 1 01 = 2 10 = 4 11 = 8
4	1	agc_adapt_ena	AGC adaption enable: 0 = freeze adaption 1 = activate adaption

Table 13. Equalizer & AGC, Register #5 (Address A<3:0>=0101) (Continued)

Bit	Default	Mnemonic	Description
3:2	0.0	agc_adapt_gain	AGC adaption step size: 00 = 1 01 = 2 10 = 4 11 = 8
1	1	afe_ena	Analog front end enable (also enables matching filter oscillator core): 0 = disabled (no bias) 1 = enabled
0	0		

Table 14. Matching Filter 2, Register #6 (Address A<3:0>=0110)

Bit	Default	Mnemonic	Description
7:5	0.1.0		Not for customer use
4:3	1.0		Not for customer use
2:1	0.0		Not for customer use
0	1		Not for customer use

1. This register is used in CMI (co-ax) mode only.

Table 15. Slicer, Register #7 (Address A<3:0>=0111)

Bit	Default	Mnemonic	Description
7:4	0.0.0.0		Not for customer use
3	1	-	Unused
2	0		Not for customer use
1	0		Not for customer use
0	0		Not for customer use

Table 16. RxPLL 1, Register #8 (Address A<3:0>=1000)

Bit	Default	Mnemonic	Description
7:5	0.1.1		Not for customer use
4:3	0.0		Not for customer use
2	0		Not for customer use
1	0		Unused
0	1		Not for customer use

Table 17. Rx PLL 2, Register #9 (Address A<3:0>=1001)

Bit	Default	Mnemonic	Description
7	1		Not for customer use
6	1		Not for customer use
5:3	0.1.1	freq_det_pw	Frequency detector output pulse width ({1 to 8} * 6.43 ns)
2	1		Not for customer use
1	1		Not for customer use
0	1		Not for customer use

Table 18. Test, Register #10 (Address A<3:0>=1010)

Bit	Default	Mnemonic	Description
7	1	los_clk_ena	Enables Rx clock switching under LOS/$\overline{\text{LOCK}}$ condition: 0 = disable 1 = enable
6	0		Not for customer use
5:2	0.0.0.0		Not for customer use
1	1		Not for customer use
0	0		Not for customer use

Table 19. Register, Bias and Fuse Controls, Register #11 (Address A<3:0>=1011)

Bit	Default	Mnemonic	Description
7	0	bias_pwrdn	Power down all bias generators. This bit can be used to power down all the active analog circuitry on the device. 0= active 1=power down
6	1	reg_reset	Register array $\overline{\text{reset}}$, ignores remainder of transaction (active low). This register is write only.
5:2	1.0.0.0		Not for customer use
1:0	0.0		Not for customer use

Table 20. Rx Digital 1, Register #12 (Address A<3:0>=1100)

Bit	Default	Mnemonic	Description
7	0	los_format	Combine (logical OR) LOS/LOCK function onto LOS pin: 0 = disable 1 = enable
6	1	los_amp_trim	Amplitude LOS threshold trim: 0 = Reduced ALOS dessert threshold (-3db) 1 = Nominal ALOS thresholds

Table 20. Rx Digital 1, Register #12 (Address A<3:0>=1100) (Continued)

Bit	Default	Mnemonic	Description
5:4	1.1	los_ena	LOS disable controls (amplitude LOS & digital LOS): 0 = disable 1 = enable
3	0	frame_ena	Byte align enable: If used, this feature must be enabled during system configuration prior to applying data to the receiver. If this is not possible see application note AN141 for further details. 0 = byte align disabled 1 = byte align enabled
2	0		Not for customer use
1	0		Not for customer use
0	1		Not for customer use

.

Figure 15. Rx Digital 2, Register #13 (Address A<3:0>=11001)

Bit	Default	Mnemonic	Description
7	1	rx_dig_reset	Rx digital circuitry reset. This can be used to minimize power comsumption when the device is disabled but not powered down. It must be enabled when the device is active 0 = reset 1 = normal operation
6:3	0.0.0.0	cnffp	Frame pulse position. Refer to figure 5 for usage.
2:1	1.0	los_tran_assert	D-LOS transition density count for assertion: 00 = 128 01 = 512 10 = 3112 11 = 4096 A-LOS assertion integration period: 00 = 2048 bits 01 = 512 bits 10 = 128 bits 11 = 32 bits
0	1	los_tran_deassert	D-LOS transition density count for de-assertion: 0 = 4/32 1 = SONET compliant[1] A-LOS de-assertion integration period: 0 = 0 bits 1 = 128 bits

1. SONET compliant LOS de-assertion refers to Bellcore GR-253, pages 6-16 (section 6.2.1.1.1), recommendation R6-54, LOS alarm is de-asserted (cleared) when two valid frame headers have been received with no LOS events in the interval.

.

Table 21.   Status Control, Register #14 (Address A<3:0>=1110)

Bit	Default	Mnemonic	Description
7:4	0.0.0.0	-	Unused
3:0	0.0.0.0	stat_cont	Status register (register #15) mux control (indirect addressing to increase read space)

Table 22. Read-only Register #15 (Address A<3:0>=1111)

Value of: stat_cont	Status Output							
	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
00 (Status register)	Analog LOS	Digital LOS	Tx clock activity alarm status	SONET OOF signal	Unused[3]		Rx PLL frequency lock alarm	Unused[3]
01	Not for customer use			Not for customer use				
02	Not for customer use			Not for customer use				
03 (Fuse contents-upper bits)	Not for customer use							
04 (Fuse contents-upper bits)	Not for customer use				Not for customer use			
05[1,2] (Interrupt register)	Analog LOS interrupt (los_ana_i)	Digital LOS interrupt (los_dig_i)	Tx clock alarm interrupt	OOF interrupt (oof_i)	Unused[3]	Unused[3]	Rx PLL frequency lock alarm interrupt (rx_lock_i)	CMI coding error alarm interrupts (cmi_err_i)
06[4] (Device ID)	MSB							LSB

1. Bits 7:1 are cleared upon reading the status register (stat_cont = 00).
2. Bit 0 is cleared upon reading interrupt register (stat_cont = 05).
3. Ignore these bits during register transactions, unpredictable contents
4. Contains device revision number in hexadecimal notation.

4.0   Application Information

The following provides application examples of interfacing the LXT6155 to the line side and the overhead terminator side. Line side encoding schemes can be one of two types: LVPECL NRZ encoded for a fiber optic module, or CMI encoded for a 75Ω coax cable. On the systems side, serial differential or parallel eight-bit modes can be used. All signals are TTL level compatible, except serial interface signals (TPOS, TNEG, TSICLKP, TSICLKN, RSOCLKP, RSOCLKN, RPOS, and RNEG) which are 3.3V LVPECL compatible.

4.1   Fiber Optic Module Interface

The LXT6155 is designed to directly drive a 3.3V LVPECL fiber optic transceiver. The LVPECL drivers require the proper transmission line impedance to correctly drive the fiber module. Signal traces should be 50 Ω controlled impedance lines and should be biased to the appropriate level. Please refer to Figure 16 for the proper interface.

To interface the LXT6155 LVPECL signals to a 5V PECL fiber optic module, please refer to the LXT6155 application note AN141.

4.2   Coax Interface

As shown in 17 on page 35, the LXT6155 directly drives a transformer connected to a 75 Ω coaxial cable, up to12.7dB cable loss at 78MHz. This is approximately 110m of RG59U. Please refer to manufacturers specifications for maximum cable lengths. Output CMI waveform conform to the ITU G.703 specifications. Rise and fall times are less than 2.0 ns.

Figure 16. 3.3 V LVPECL to 3.3 V LVPECL Interface
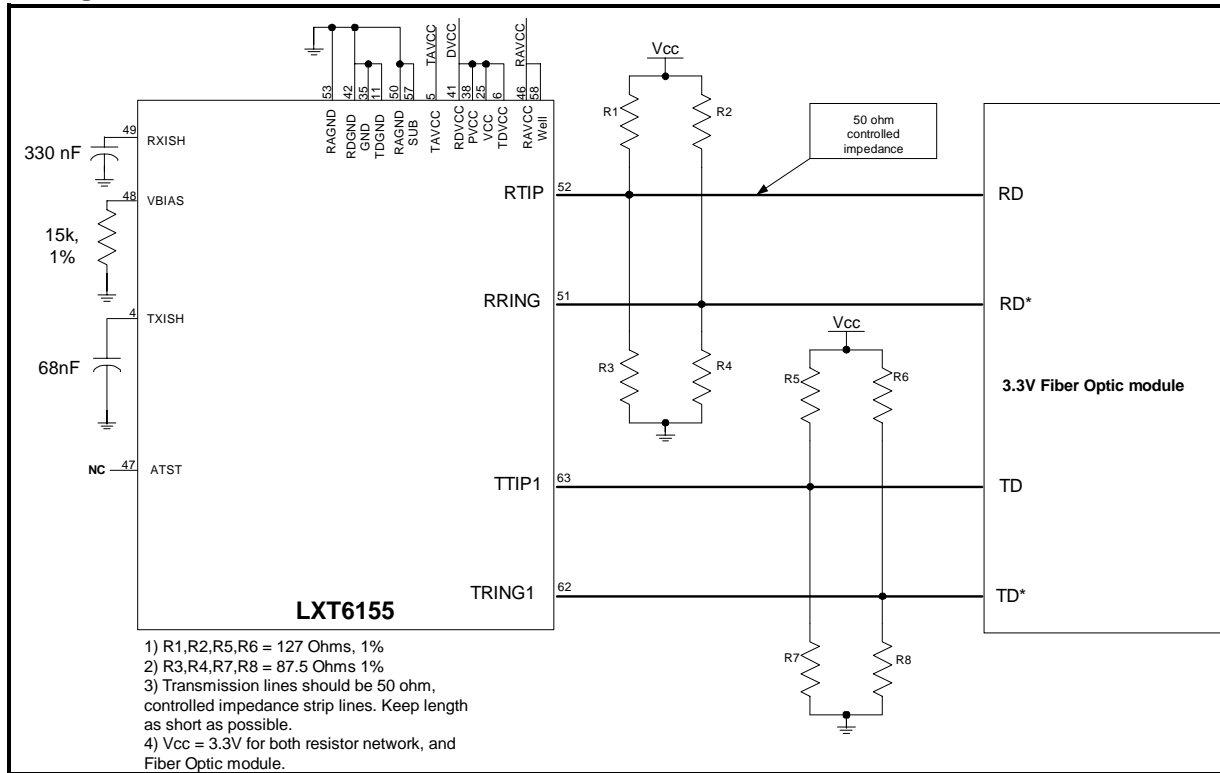

1) R1,R2,R5,R6 = 127 Ohms, 1%
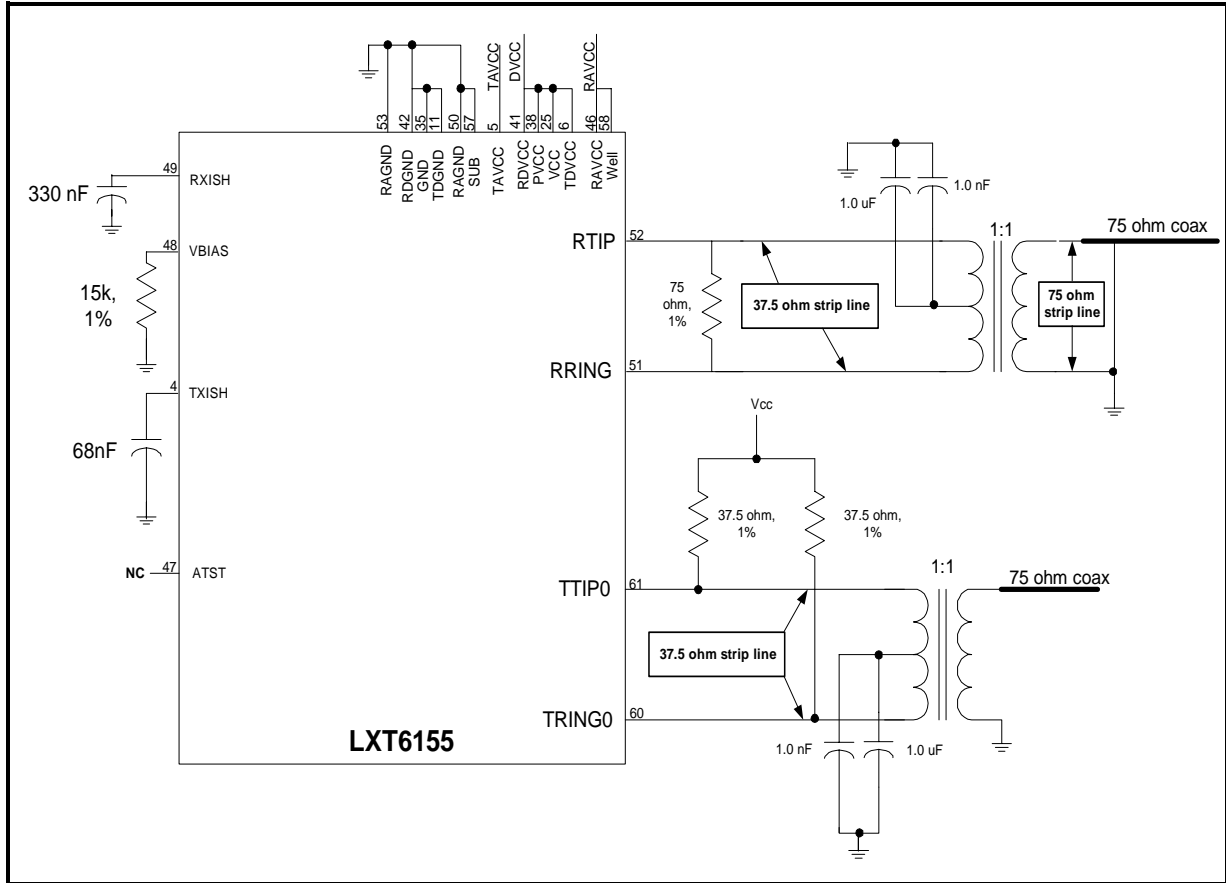2) R3,R4,R7,R8 = 87.5 Ohms 1%
3) Transmission lines should be 50 ohm, controlled impedance strip lines. Keep length as short as possible.
4) Vcc = 3.3V for both resistor network, and Fiber Optic module.

Figure 17. 75 Ω Coax Cable Interface

Table 23. Transformer Specifications

Parameter		Min	Typ	Max	Unit	Notes
Transmission, S12	-3dB Low			10	MHz	
	-3dB High	320		-	MHz	
Return Loss, S11	-20dB Low			5	MHz	
	-20dB High	250		-	MHz	
In-band Loss				0.5	dB	30 MHz ~ 300 MHZ
Common mode rejection				-10	dB	DC~250MHz
Cross-talk in dual packages				-40	dB	DC~156MHz
Turns ratio		0.97	1.0	1.03		

Table 24. Crystal Specifications

Parameter	Min	Typ	Max	Unit	Notes
Center frequency		19.44		MHz	
Freq tolerance	-20		20	ppm	At 25°C
Temperature drift	-20		20	ppm	-40 ~ 85°C
Aging	-10		10	ppm	First 10 years
Mode		Fundamental			
Shunt capacitance			5	pF	
Equivalent resistance		8.4		W	
Temperature Range	-40		85	$^\circ$C	

5.0 Test Specifications

Information in Table 25 through 34 and Figures 18 through 28 represent the performance specifications of the LXT6155 and are guaranteed by test, except as noted by design.

Table 25. Absolute Maximum Ratings

Parameter	Sym	Min	Max	Unit
DC supply (reference to GND)	Vcc		4.0	V
Input voltage, TTL pins	Vin (TTL)	GND -0.3	5.5	V
Input voltage, other pins	Vin	GND -0.3	Vcc +0.3	V
Input current, any pin	Iin	-10	25	mA
Storage temperature	Tstg	-65	150	°C
CAUTION Operating at or beyond these limits may result in damage to the device. Normal operation not guaranteed at these extremes.				

Table 26. Recommended Operating Conditions

Parameter		Sym	Min	Typ	Max	Unit
DC supply (referenced to GND)		Vcc	3.0	3.3	3.6	V
Ambient operating temperature		Ta	-40	25	85	°C
Total current consumption	serial/fiber				150	mA
	serial/coax				210	
	parallel/fiber				100	
	parallel/coax				150	

Table 27. DC Electrical Characteristics (Vcc = 3.0 V to 3.6 V; TA = -40 °C to 85 °C)

Parameter	Sym	Min	Typ[1]	Max	Unit	Test Conditions
High level input voltage (LVPECL)	Vih1	Vcc-1.03		Vcc-0.88	V	
Low level input voltage (LVPECL)	Vil1	Vcc-1.81		Vcc-1.62	V	
High level output voltage (LVPECL)	Voh1	Vcc-1.03	Vcc-0.95	Vcc-0.88	V	50 Ω pulled down to Vcc -2.0 V.
Low level output voltage (LVPECL)	Vol1	Vcc-1.81	Vcc-1.70	Vcc-1.62	V	
High level input voltage (TTL)	Vih2	2.0			V	
Low level input voltage (TTL)	Vil2			0.8	V	
High level output voltage (TTL)	Voh2	2.4			V	IOH = 4 mA
Low level output voltage (TTL)	Vol2			0.4	V	IOL = 4 mA
Input leakage current, low (TTL)	Ill			10	µA	
Input leakage current, high (TTL)	Ilh			10	µA	
1 Typical values are at 25C and 3.3V. They are for design aid only; not guaranteed and not subject to production testing.						

Table 28. Transmit Timing Characteristics (See Figures 18 and 19)

Parameter	Sym	Min	Typ[1]	Max	Unit	Test Conditions
Transmit serial input clock frequency			155.52		MHz	
Transmit serial input clock frequency error		-20		+20	ppm	Compliant with GR253
Transmit serial input clock duty cycle		45		55	%	
Transmit serial input clock and data rise /fall time[2]				1.2	ns	20% - 80%
Transmit parallel input clock frequency			19.44		MHz	
Transmit parallel input clock frequency error		-20		+20	ppm	
Transmit parallel input clock duty cycle		45		55	%	
Transmit parallel input data & clock rise/fall time[2]		2		10	ns	
TPICLK to TPID<0:7> hold time	Thtpid	3			ns	
TPICLK to TPID<0:7> setup time	Tstpid	2			ns	
TSICLKP(TSICLKN) to TPOS (TNEG) setup time	Tstpos	1.25			ns	
TSICLKP (TSICLKN) to TPOS (TNEG) hold time	Thtpos	0.75			ns	

1. Typical values are at 25C and 3.3V. They are for design aid only; not guaranteed and not subject to production testing.
2. Not production tested, guaranteed by design and other correlation factors.

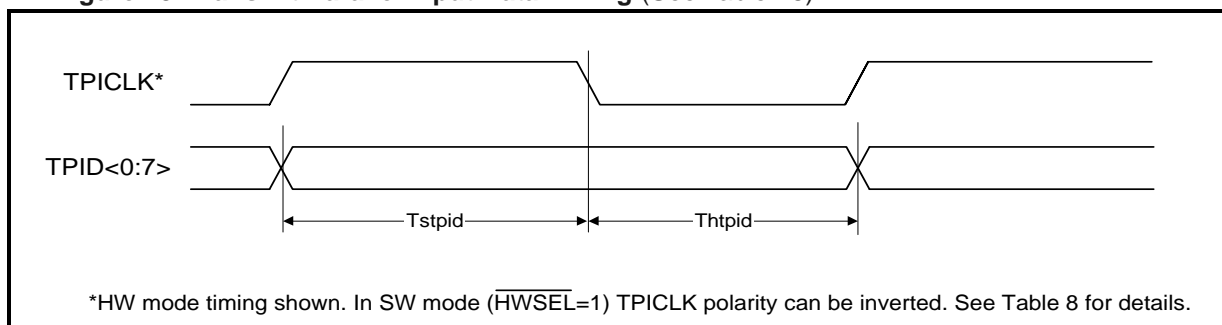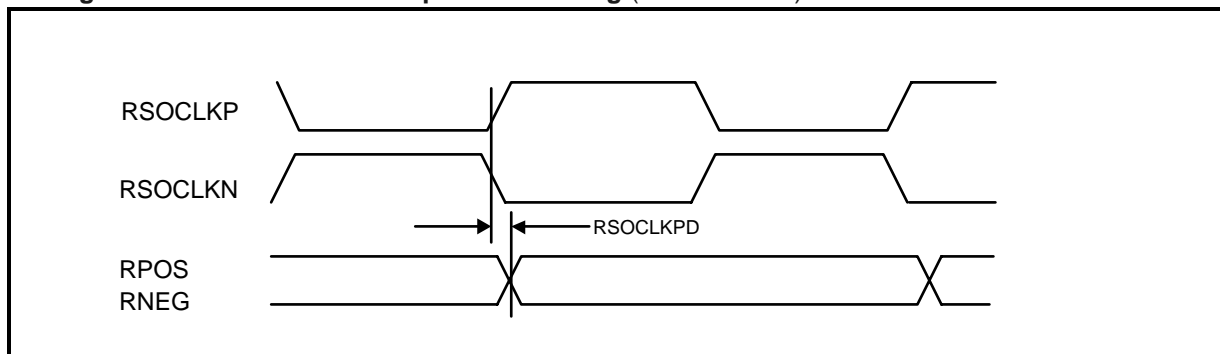**Figure 18. Transmit Parallel Input Data Timing** (See Table 28)

*HW mode timing shown. In SW mode (HWSEL=1) TPICLK polarity can be inverted. See Table 8 for details.

Figure 19. Transmit Serial Input Data Timing (See Table 28)
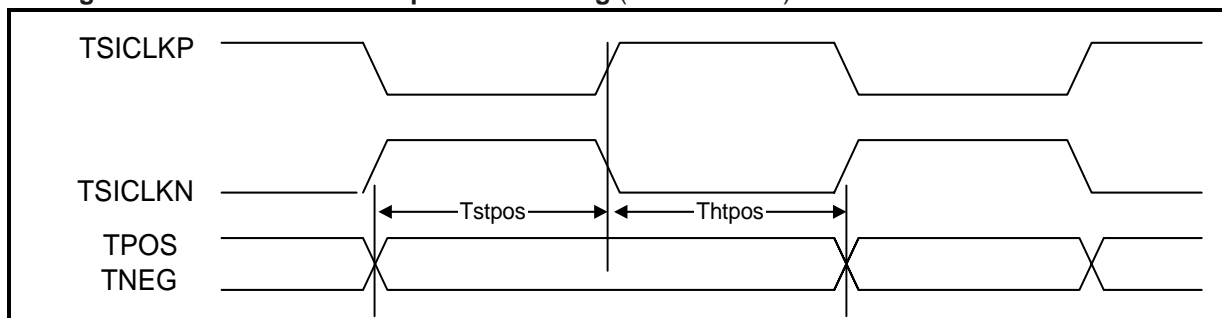
Table 29. Transmit Analog Characteristics

Parameters	Note	Min	Typ[1]	Max	Unit	Test Conditions
Transmit jitter generation[2] (Intrinsic jitter SONET spec)	12 kHz - 1.3 MHz			0.1	UIpp	PRBS(23) pattern. Transmit input data and clock have no input jitter. Receive line input is all zeros.
				0.01	UIrms	
Transmit jitter generation[2] (Intrinsic jitter SDH spec)	500 Hz - 1.3 MHz			1.5	UIpp	
	65 kHz - 1.3 MHz			0.075	UIpp	
Transmit jitter transfer function peaking[2]	DC - 230 kHz			0.4	dB	PRBS(23) data. Input jitter as shown in Figure 26.
Synthesizer capture range	Fcap	-20		+20	ppm	
Synthesizer track range	Ftrack	-20		+20	ppm	parallel mode
Synthesizer lock time	Tlock			100	µs	
Transmit output rise and fall times - CMI signals	TTIP0 TRING0			2.2	ns	10% - 90% 0m cable length
Transmit output amplitude - CMI signals	TTIP0 TRING0	0.9		1.1	Vpp	
TTIP0/TRING0 output impedance	Zout	1.6	2.0		kΩ	

1. Typical values are at 25C and 3.3V. They are for design aid only; not guaranteed and not subject to production testing.
2. Not production tested, guaranteed by design and other correlation factors.

Table 30. Receive Timing Characteristics (See Figures 20 and 21)

Parameter	Sym	Min	Typ[1]	Max	Unit	Test Conditions
Receive serial output clock frequency	RSOCLKp RSOCLKn		155.52		MHz	
Receive serial output clock duty cycle	RSOCLkdc	45		55	%	
Receive serial output clock and data rise/fall time[2]	-			1.2	ns	20% - 80%.
RSOCLKP/RSOCLKN to RPOS/ RNEG propagation delay	RSOCLKpd	-0.5		1.5	ns	
Receive parallel output clock frequency	RPOCLK		19.44		MHz	
Receive parallel output clock duty cycle	RPOCPdc	45		55	%	
Receive parallel output data & clock rise/fall time	RPOCLKt	2		5	ns	
RPOCLK to RPOD<0:7> propagation delay	RPOCLKpd	0		7	ns	
RPOCLK to ROFP propagation delay	ROFPpd	0		4	ns	
Reference Input Clock into XTALIN pin (TTL)	REFCLK		19.44		MHz	The REFCLK replaces the crystal

1. Typical values are at 25C and 3.3V. They are for design aid only; not guaranteed and not subject to production testing.
2. Not production tested, guaranteed by design and other correlation factors.

Table 30. Receive Timing Characteristics (See Figures 20 and 21) **(Continued)**

Parameter	Sym	Min	Typ[1]	Max	Unit	Test Conditions
Reference Clock Offset from Nominal		-100		100	ppm	
1. Typical values are at 25C and 3.3V. They are for design aid only; not guaranteed and not subject to production testing. 2. Not production tested, guaranteed by design and other correlation factors.						

Figure 20. Receive Serial Output Data Timing (See Table 30)

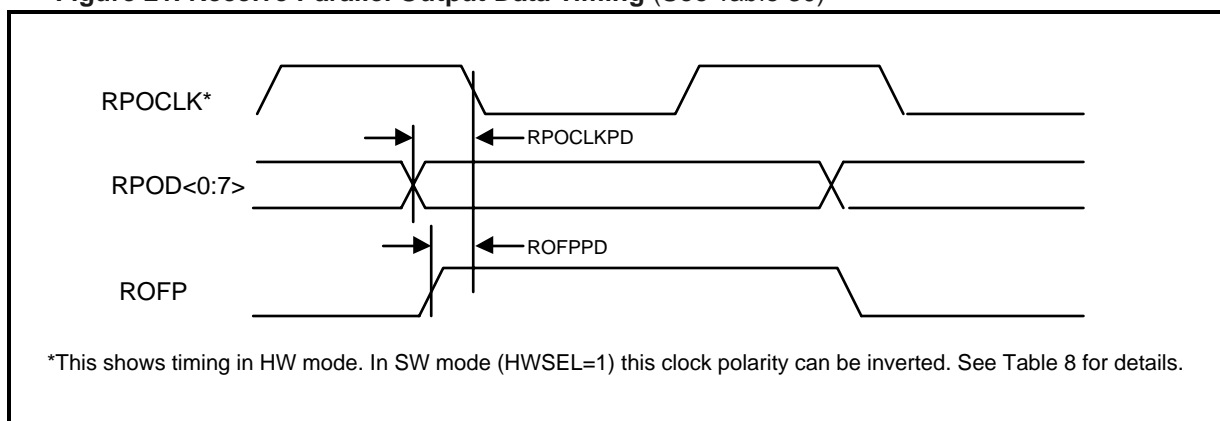**Figure 21. Receive Parallel Output Data Timing** (See Table 30)

*This shows timing in HW mode. In SW mode (HWSEL=1) this clock polarity can be inverted. See Table 8 for details.

Table 31. Receive Analog Characteristics

Parameter	Note	Min	Typ[1]	Max	Unit	Test Conditions
End to end loss budget (coax)[1]	-	15			dB	BER=1E-12. PRBS (23) data. CMI encoded. Input white noise = 5 mV RMS max.
LOS - fiber	Assert		20		μsec	No data transition. Default LOS setting.
	De-assert		187.5		μsec	No LOS events. Default LOS settings.
1. Typical values are at 25C and 3.3V. They are for design aid only; not guaranteed and not subject to production testing. 2. Not production tested, guaranteed by design and other correlation factors.						

Table 31. Receive Analog Characteristics (Continued)

Parameter	Note	Min	Typ[1]	Max	Unit	Test Conditions
LOS Thresholds - Coax	Assert	18			dB	Attenuation measured at 78 MHz, CMI, 75 Ω load. 12.7 dB cable loss plus remaining flat loss.
	De-assert	17			dB	
LOS hysteresis - coax	HYS	1.0		4.0	dB	Measured from the level where LOS is asserted. PRBS(23) data.
Receive jitter generation[2] (intrinsic jitter SONET spec)	12 kHz - 1.3 MHz			0.01	UIrms	CMI encoded PRBS(23) at RTIP/RRING with no data jitter. Transmit input = all zeros Refer to Figure 27 and Table 33.
				0.1	UIpp	
Receive jitter generation[2] (intrinsic jitter SDH spec)	500 Hz - 1.3 MHz			1.5	UIpp	
	65 kHz - 1.3 MHz			0.075	UIpp	
Receive jitter transfer peaking[2]	DC - 230 kHz			0.4	dB	PRBS(23) Data. Input jitter as the max. tolerance curve shown in Figure 26.
Receive jitter tolerance[2]	0.1 Hz - 19.3 Hz	39			UIpp	BER=1E-10. Tolerated jitter meets Figure 26
	500 Hz - 6.5 kHz	1.5			UIpp	
	65 kHz -	0.15			UIpp	
PLL nominal center frequency	Fnom		155.52		MHz	
PLL capture range	Fcap	-20		+20	ppm	
PLL track range	Ftrack	-20		+20	ppm	
PLL lock time	Tlock		100		μs	PRBS(23) pattern, from data applied at RTIP/RRING. Device in fiber optic mode.
Equalizer adaptation time			500		bits	From data applied
Line input impedance (RTIP and RRING)	RIN	4			kΩ	Differential resistance

1. Typical values are at 25C and 3.3V. They are for design aid only; not guaranteed and not subject to production testing.
2. Not production tested, guaranteed by design and other correlation factors.

Parameter	Sym	Min	Typ	Max	Unit	Test Conditions[1]
Rise/Fall time - All TTL outputs	tRF			25	ns	Load 1.6mA, 50pF
SDI to SCLK setup time	tDC	5			ns	
SCLK to SDI hold time	tCDH	5			ns	
SCLK low time	tCL	120			ns	
SCLK high time	tCH	120			ns	
SCLK rise and fall time	tR, tF			25	ns	
$\overline{CS}$ to SCLK setup time	tCC	5			ns	
SCLK to $\overline{CS}$ hold time	tCCH	5			ns	
$\overline{CS}$ inactive time	tCWH	5			ns	
SCLK to SDO valid	tCDV	0		20	ns	

1. Typical values are at 25C and 3.3V. They are for design aid only; not guaranteed and not subject to production testing.

Parameter	Sym	Min	Typ	Max	Unit	Test Conditions[1]
SCLK falling edge to SDO high Z	tCDZ	0		20	ns	
CS rising edge to SDO high Z	tCZ	0		20	ns	

1. Typical values are at 25C and 3.3V. They are for design aid only; not guaranteed and not subject to production testing.
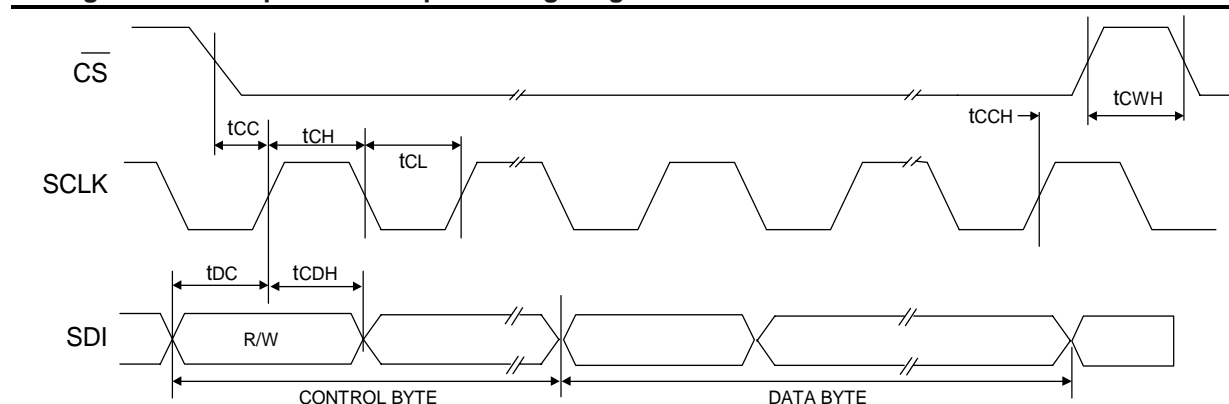
Figure 22. Microprocessor Input Timing Diagram

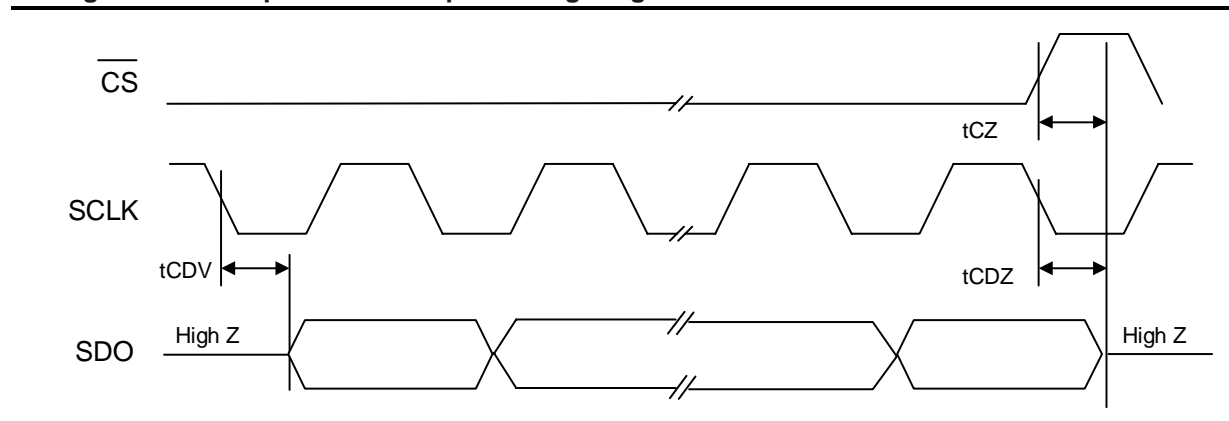**Figure 23. Microprocessor Output Timing Diagram**
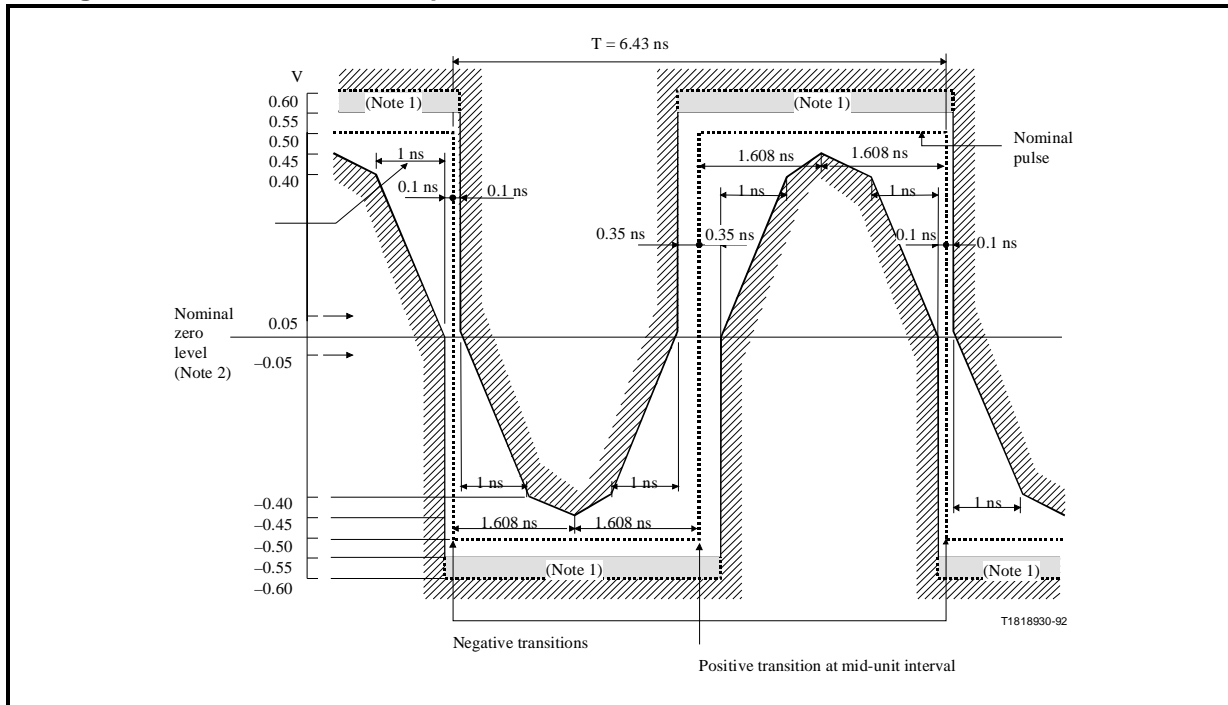
Figure 24. CMI Encoded Zero per G.703 and STS-3

Figure 25. CMI Encoded One per G.703 and STS-3
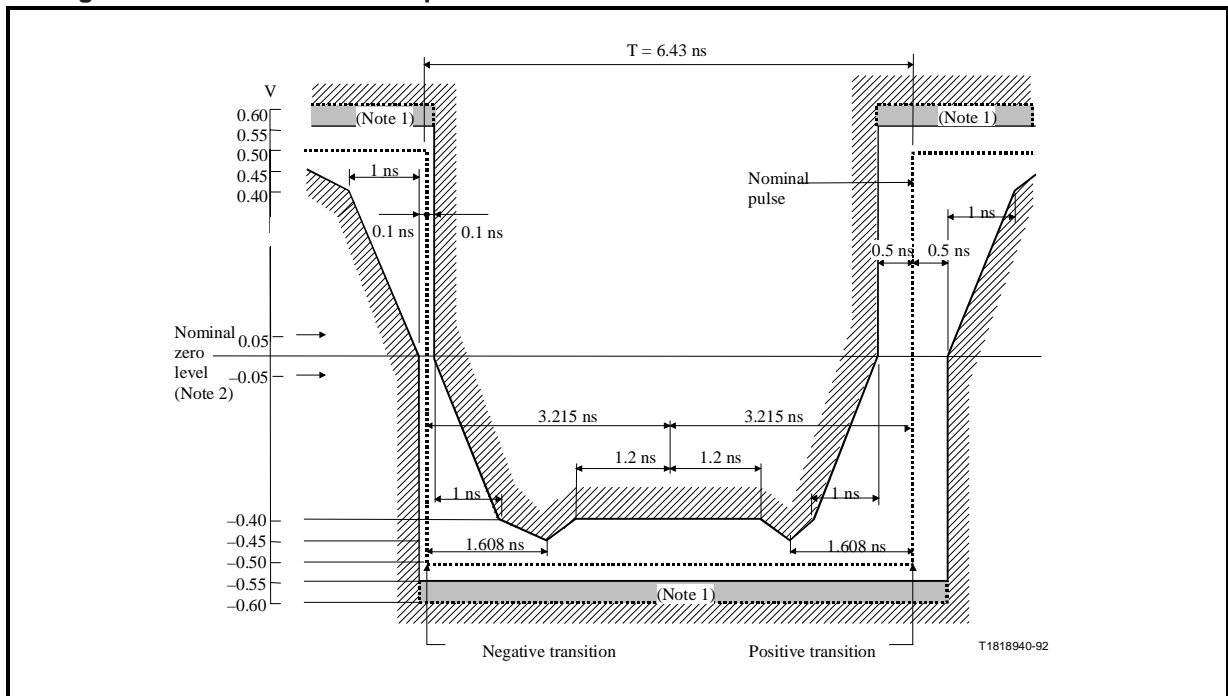
Note: *The maximum "steady state" amplitude should not exceed the 0.55 V limit. Overshoots and other transients are permitted to fall into the dotted area.*

Note: *With the signal applied, the vertical position of the trace can be adjusted with the objective of meeting the limits of the masks. Any such adjustment should be the same for both masks and should not exceed ±0.05 V.*

Table 32. Jitter Tolerance (in UIpp)

Frequency	OC3	STM1
10 Hz	15	
19.3 Hz		39
30 Hz	15	
300 Hz	1.5	
500 Hz		1.5
6.5 kHz	1.5	1.5
65 kHz	0.15	0.15
1.3 MHz	0.15	0.15

Figure 26. Jitter Tolerance
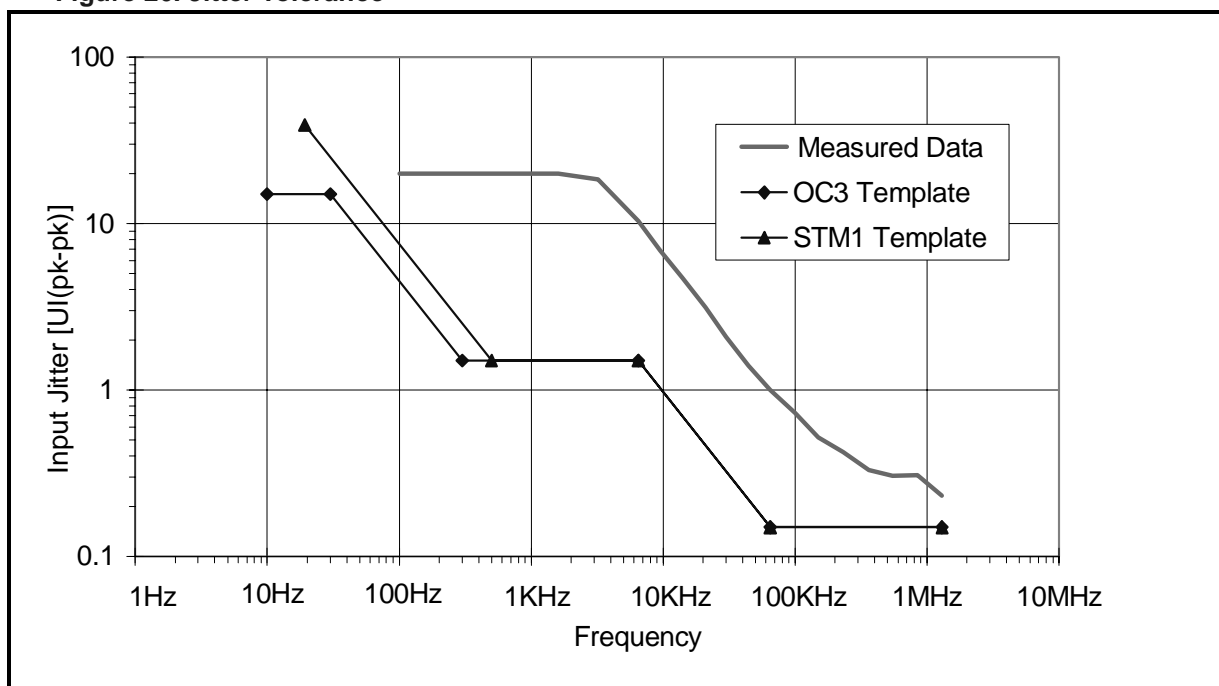
Table 33. Jitter Generation

Signal	f1	f2	Measured Jitter
OC3	12 kHz	1.3 MHz	0.01 UI rms
			0.1 UIpp
STM1	500 Hz	1.3 MHz	1.5 UIpp
	65 kHz	1.3 MHz	0.075 UIpp

Table 34. Jitter Transfer

Signal	f1	A1	Unit
OC3	230 kHz	0.4	dB
STM1	230 kHz	0.4	dB

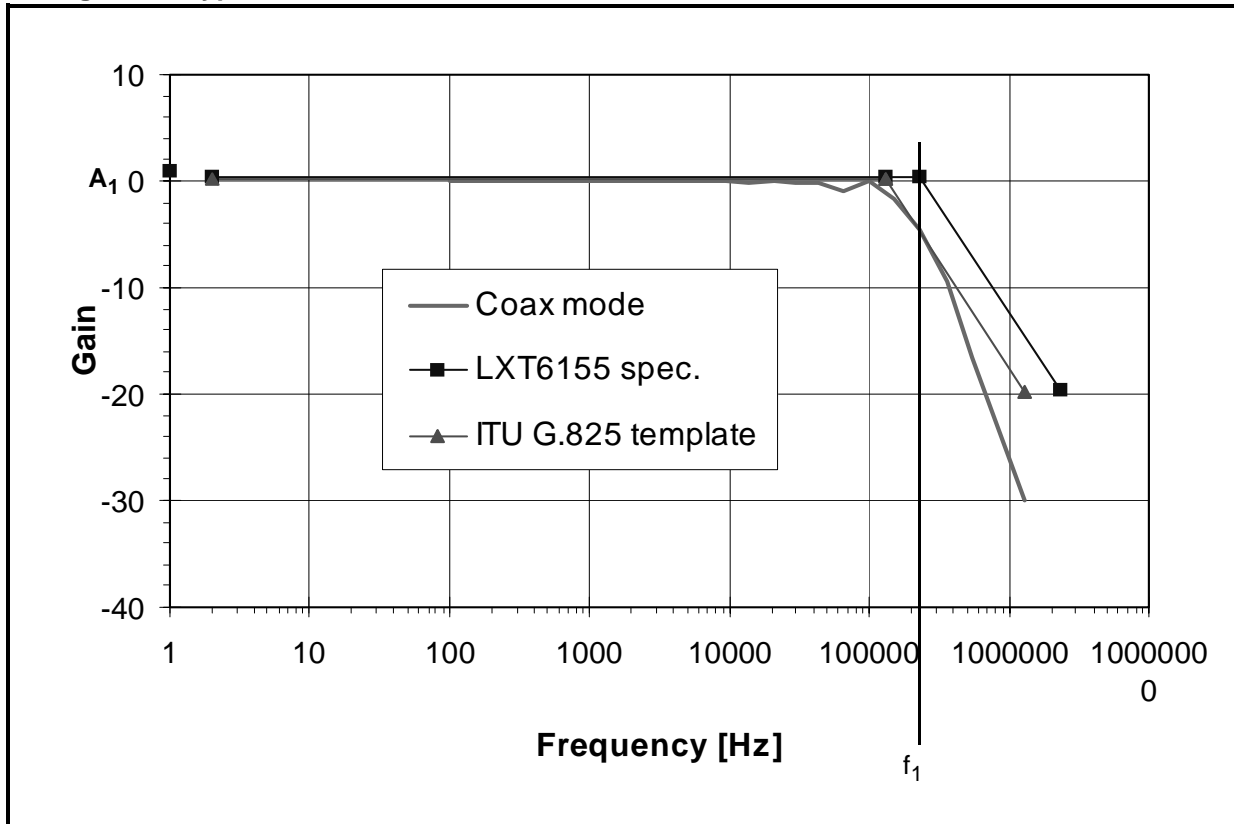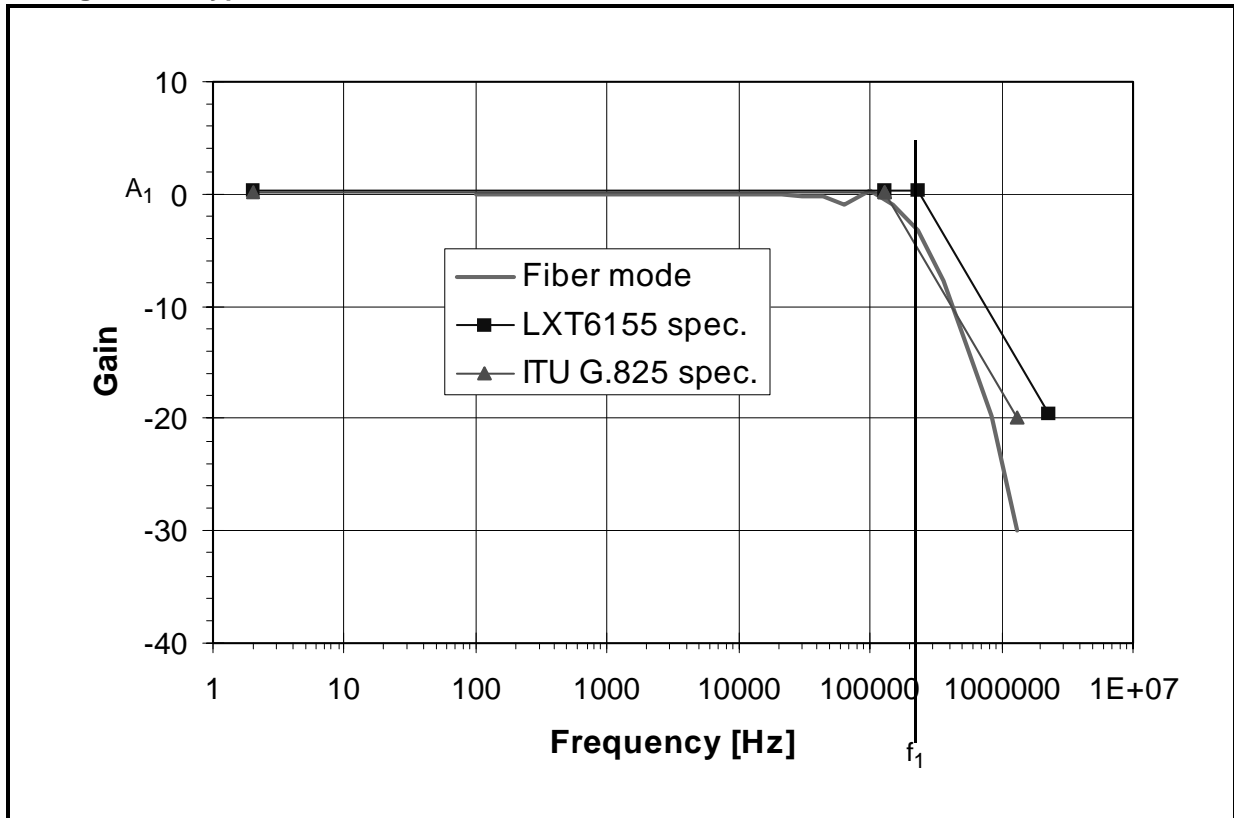**Figure 27. Generation Measurement Filter Characteristics**
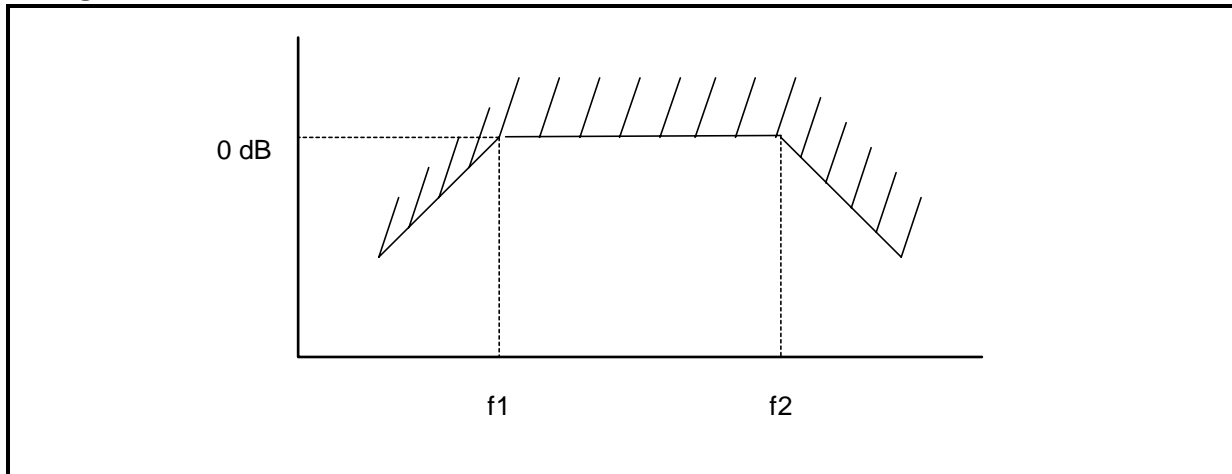
Figure 28. Typical Coax Jitter Transfer

Note: Measured with the device in remote loopback. Data reflects total jitter in both Tx and Rx path
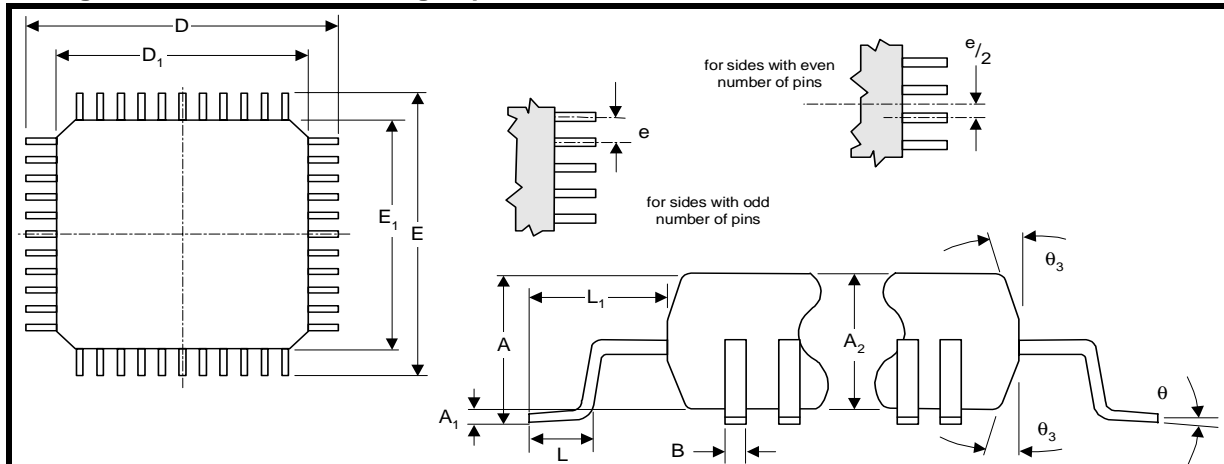
Figure 29. Typical Fiber Jitter Transfer

Note: Measured with the device in remote loopback. Data reflects total jitter in both Tx and Rx path

6.0   Mechanical Specifications

Figure 30. LXT6155LE Package Specification

64-pin Low-profile Quad Flat Pack

— Part Number LXT6155LE

— Extended Temperature Range: -40° to 85 °C

Dim	Inches		Millimeters	
	Min	**Max**	**Min**	**Max**
A		.063		1.60
A1	.002	.006	0.05	0.15
A2	.053	.057	1.35	1.45
B	.007	.011	0.17	0.27
D	0.472 BSC[1]		12.00 BSC[1]	
D1	0.394 BSC[1]		10.00 BSC[1]	
E	0.472 BSC[1]		12.00 BSC[1]	
E1	0.394 BSC[1]		10.00 BSC[1]	
e	0.020 BSC[1]		0.50 BSC[1]	
L	0.018	0.030	0.45	0.75
L1	0.039 REF		1.00 REF	
θ3	11°	13°	11°	13°
q	0°	7°	0°	7°
1. BSC—Basic Spacing between Centers				