± 3 digit A/D converter

designed for . . .

- **Digital Voltmeters, Panel Meters**
- **Digital Thermometers**
- **General Instrumentation (Noise, Light, pH, etc.)**
- **Microprocessor Interfaces to Analog Signals**

Siliconix

BENEFITS

- Accuracy of 0.1% ±1 Count For Full Use of 3 Digits
- Low Power Consumption of 25 mW
- Minimum External Parts Count
- Auto-Zero and Auto-Polarity
- Buffered Signal and Reference Inputs ($Z_{IN} > 10^9\ \Omega$)
- Internal Oscillator Uses Only One External Capacitor
- Wide Sampling Range of 1 to 60/Second
- Multiplexed BCD Output For Simple Display and μ-P Interface

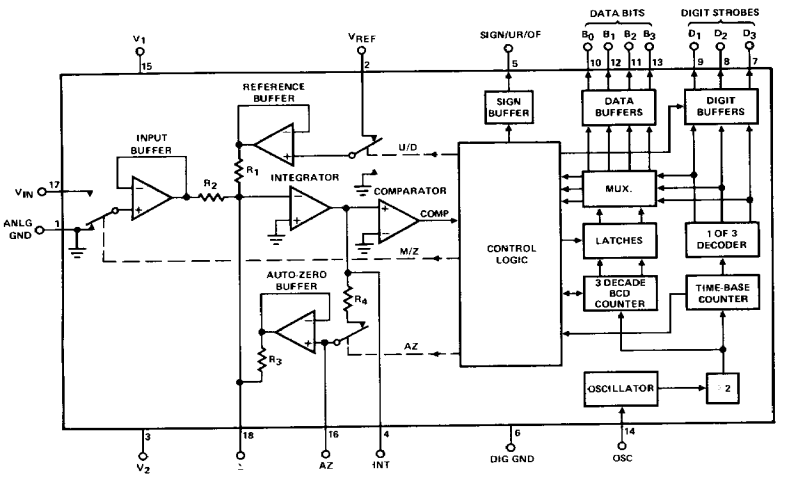
DESCRIPTION

The LD130 combines both the analog and digital subsystems of a 3 digit A/D system in a single monolithic CMOS I.C. The "Quantized Feedback" conversion scheme, introduced by Siliconix, provides the LD130 with an Auto-Zero, Auto-Polarity A/D system requiring only a single reference voltage. External parts are minimized by the on-chip resistors and buffer amplifiers. These high impedance input and reference buffer amplifiers eliminate source loading errors providing the outstanding temperature coefficient and ratio operation inherent in this system. Break-before-make switch action insures that neither the analog input nor the reference voltage will be shorted to ground at any time.

The LD130 3 digit A/D is made functionally complete by the following additions:

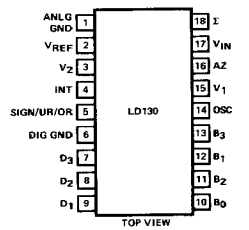
1. C_{AZ} (0.10 μF) between AZ and Σ pins
2. C_{INT} (0.033 μF) between INT and Σ pins
3. C_{OSC} (0.001 μF) between OSC and Digital Ground
4. $V_{REF} \cong 2.000$ V
5. ±5 V supplies (@ 3 mA)

FUNCTIONAL DIAGRAM



PIN CONFIGURATION

Dual-In-Line Package



ORDER NUMBER LD130CJ
SEE PACKAGE 19

ABSOLUTE MAXIMUM RATINGS

V_{IN}	$V_1 + 0.3$ V, $V_2 - 0.3$ V
$V_1 - V_2$	16 V
V_1	8 V
Current at V_{IN}	1 mA
Voltage on any pin	$V_1 + 0.3$ V, $V_2 - 0.3$ V
V_{REF}	V_1
Operating Temperature (BP)	−20 to 85°C
Operating Temperature (CJ)	0 to 70°C
Storage Temperature (C Suffix)	−65 to 125°C
Power Dissipation* (J Package)	450 mW
Power Dissipation (P Package)	1000 mW

*Device mounted with all leads welded or soldered to PC Board, Derate 6.3 mW/°C above 25°C.

Absolute Maximum Ratings are stress limits only. Exceeding these limits may cause device damage. Electrical Characteristics define the functional operating limits.

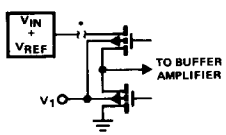
ELECTRICAL CHARACTERISTICS

All DC parameters are 100% tested at 25°C. Lots are sample tested for AC parameters and High Temperature Limits to assure conformance with specifications.

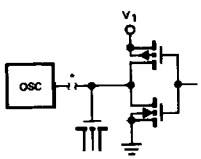
		CHARACTERISTIC		MIN	TYP	MAX	UNIT	TEST CONDITIONS $V_1 = +5$ V, $V_2 = -5$ V, $V_{REF} = 2.000$ V, $T_A = 25°C$, $C_{INT} = 0.033\ \mu F$, $C_{strg} = 0.1\ \mu F$
1	GENERAL		Linearity			0.1	% rdg	
2	GENERAL		Noise		0.3		LSB	Peak-to-Peak noise apparent when going from one steady reading to another.
3	GENERAL		Zero T.C.		10		μV/°C	$0 \leq T_A \leq 70°C$
4	GENERAL		Gain T.C.		15		ppM/°C	$0 \leq T_A \leq 70°C$
5	GENERAL		NMR Normal Mode Rejection	36			dB	$f_{series} = 60$ Hz, $f_{osc} = 24$ kHz
6	INPUT	I_{IN}	V_{IN} Input Bias Current		7		pA	$T_A = 25°C$
7	INPUT	I_{IN}	V_{IN} Input Bias Current		90		pA	$T_A = 70°C$
8	INPUT	I_{REF}	V_{REF} Input Bias Current		7		pA	$T_A = 25°C$
9	INPUT	I_{REF}	V_{REF} Input Bias Current		90		pA	$T_A = 70°C$
10	INPUT	f_{CLK}	Clock Frequency		30		kHz	
11	INPUT	D.C.$_{CLK}$	Clock Duty Cycle	30/70		70/30	%	
12	INPUT	I_{INL}	Clock Input Current Low			1	mA	$V_{INL} = 0.25$ V
13	INPUT	I_{INH}	Clock Input Current High			1	mA	$V_{INH} = 4.75$V
14	OUT	V_{OL}	All Outputs			0.4	V	$I_{OL} = 1.6$ mA Over Operating Temperature Range
15	OUT	V_{OH}	Digit Strobes	2.4			V	$I_{OH} = -400\ \mu A$ Over Operating Temperature Range
16	OUT	V_{OH}	Data Bits, Sign/UR/OR	2.4			V	$I_{OH} = -100\ \mu A$ Over Operating Temperature Range
17	SUPPLY	I_1	Supply Current			6	mA	
18	SUPPLY	I_2	Supply Current			−4	mA	
19	SUPPLY	$PSRR_1$	V_1 Supply Rejection		0.6		mV/V	
20	SUPPLY	$PSRR_2$	V_2 Supply Rejection		1.4		mV/V	

Typical values are for Design Aid Only, not guaranteed and not subject to production testing. ICBG

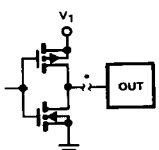
INPUT/OUTPUT SCHEMATICS



V_{IN} or V_{REF} Input



Oscillator Input

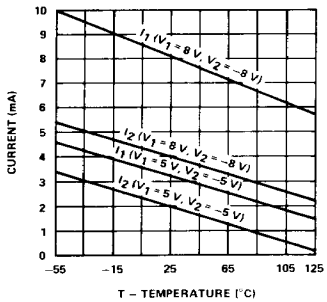


Output Buffers (Digits, Bits, SIGN/UR/OR)

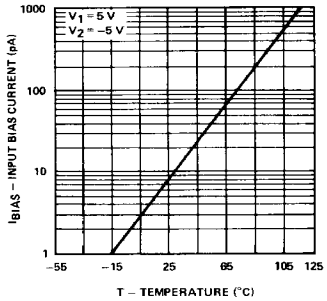
*Protection circuitry not shown.

TYPICAL CHARACTERISTICS

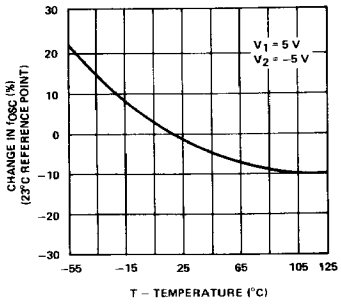
Supply Currents vs Temperature



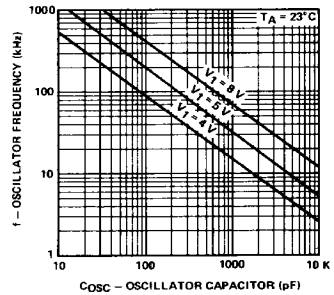
Input Bias Current vs Temperature



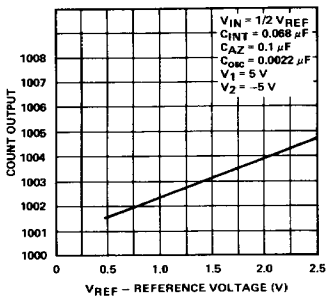
Clock Frequency vs Temperature



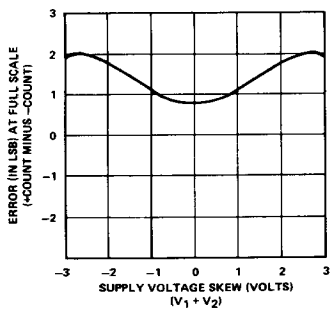
Oscillator Frequency vs C_{OSC} and V_1



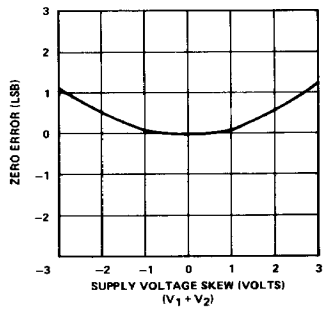
Ratio Operation (V_{IN}/V_{REF} = Constant)



Rollover Error* vs Power Supply Skew



Zero Error vs Power Supply Skew



*Difference in reading for equal + and − inputs

FUNCTIONAL OPERATION

The Connection Diagram of Figure 1 should be referred to along with the timing diagrams of Figures 2, 3, and 4 in this discussion of functional operation.

Time Base Counter – The internal oscillator circuit becomes fully functional with an external capacitor to ground. The OSC input can be driven by an external oscillator (0 to V_1 logic levels) if desired. A squaring circuit divides the oscillator frequency by two before it drives the BCD counter and Time-Base counter.

The two fundamental intervals of the sampling period, the Auto-Zero (AZ) and Measure intervals, are established by the Time-Base counter as 1024 and 2048 clock periods respectively. The total sampling interval is then 3072 clock periods long. Since the internal clock is one-half of the oscillator frequency, the sampling period is then 6144 (2 x 3072) oscillator periods. The Time-Base counter also divides the internal clock by eight. This division provides sets of eight clock periods (octets) which are used by both the data multiplexer as digit "ON" times and the control logic as U/D (Up/Down logic) duty cycle periods.

AUTO-ZERO INTERVAL

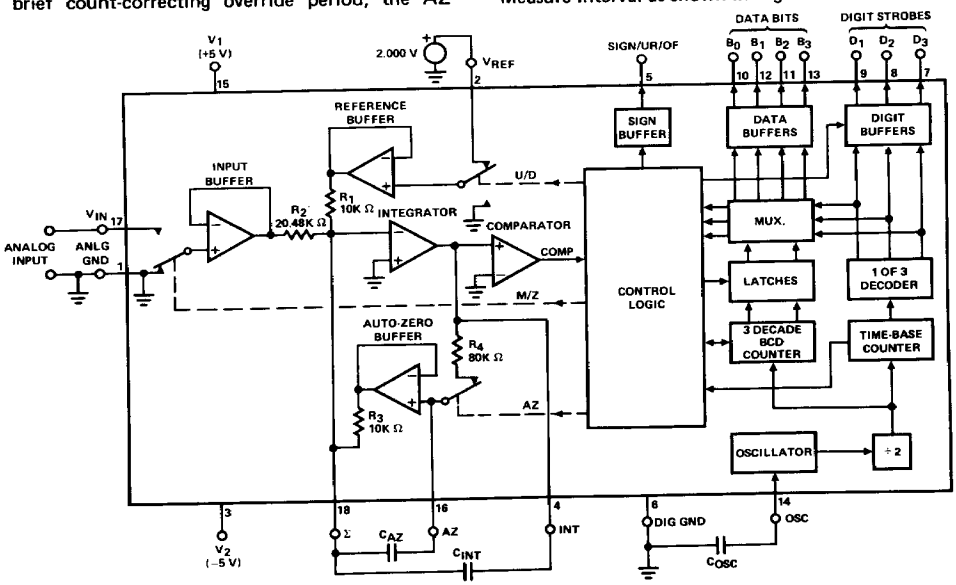
The Auto-Zero interval provides a means to null out the offset voltages of the amplifiers used in the LD130. In addition, it automatically establishes a second tracking reference voltage necessary for bi-polar A/D conversion.

The Auto-Zero sequence is initiated when the M/Z (Measure/Zero) signal switches the input buffer amp to analog ground. After a brief count-correcting override period, the AZ switch is closed connecting the AZ amplifier and Integrator together in a closed-loop second-order system. During this time the control logic ignores the comparator output and pulses the U/D switch at a 50% duty cycle of 4 clock periods "Up" and 4 "Down" (see Figure 2). Equilibrium of this closed-loop system is attained when the average currents through R_1 and R_3 are equal and opposite. This is achieved when V_{AZ}, the Auto-Zero voltage, is equal to $-\frac{1}{2} V_{REF}$ since $R_1 = R_3$. Establishing V_{AZ} and storing it on C_{AZ} gives the U/D logic the capability of switching either a + or – reference current to the integrator during conversion. Thus when U/D is "Up," $I_1 + I_3 = -V_{REF}/2R_1$ and when U/D is "Down," $I_1 + I_3 = V_{REF}/2R_1$. The Auto-Zero interval is of sufficient duration to insure that V_{AZ} will be well established.

Prior to the start of the Measure interval, the integrator output (which had been cycling around −1 V) is brought back to analog ground, the comparator threshold. The system is now ready for a conversion.

MEASUREMENT INTERVAL

The "Quantized Feedback" conversion system is characterized by a single phase Digitization interval in which a digital control system feeds back quantized units of charge in response to the sampled state of an analog comparator. These quanta of charge balance the charge being supplied to the integrator by the analog voltage. The magnitude ($V_{REF}/2R_1 \times 6/f_{clock}$) of the Quantized charge being fed back and its sign (+ or –) arise from the fact that the control logic has two U/D duty cycles available during the Measure interval as shown in Figure 3.



Connection Diagram
Figure 1

FUNCTIONAL OPERATION (Cont'd)

The U/D logic is "up" one clock cycle and "down" 7 cycles for a high comparator output in the clock cycle preceding a set of 8 cycles. This will be designated duty cycle "A." With a low comparator output in clock cycle number 7 the U/D logic will be "up" for 7 cycles and "down" for 1 cycle in the following 8 clock cycles. This is duty cycle "B." The effect of these two reference current duty cycles on the integrator output is shown in Figure 3. It can be seen that the "up" state of the U/D logic drives the integrator output voltage up. The up/down BCD counter increments by each clock pulse when the U/D logic is "up" and decrements by each clock pulse when the U/D logic is "down." Consequently the net count goes up 6 counts for a "B" duty cycle and down 6 for an "A" duty cycle.

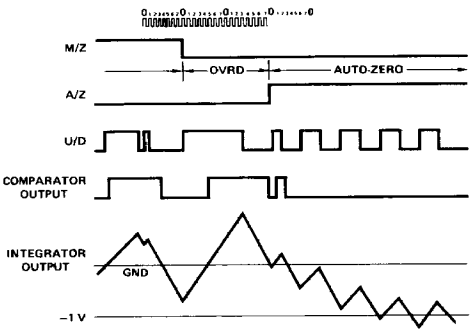
Input polarity is determined by the first appearance of two consecutive duty cycles of the same type. The control logic would determine the analog input to be negative if two "A" duty cycles occur in succession and positive if two "B" duty cycles occur in succession.

Since the counting process is done by increments (or decrements) of 6 during the measure interval, a short override interval is required at the end of the Measurement to "fine tune" the count to the nearest LSB. This occurs within the first 32 clock periods of the AZ interval.

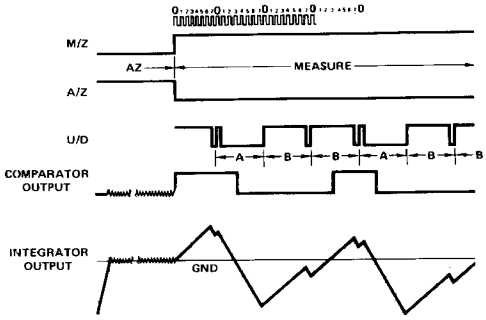
DATA FLOW

Following the count correcting override sequence; the contents of the BCD counters and sign flip-flop are loaded into the internal latches. Counter states of less than 80 or greater than 999 are decoded as underrange or overrange conditions respectively. The presence of an out-of-range signal gates a single pulse (one clock period) to the SIGN/UR/OR output during either D_1 or D_2 digit time (D_2 identifies overrange, D_1 identifies underrange). The overrange condition also provides a visual signal by holding the digit strobe outputs low during the Measure interval. This holds the display off for 2/3 of the sampling interval giving a blinking effect.

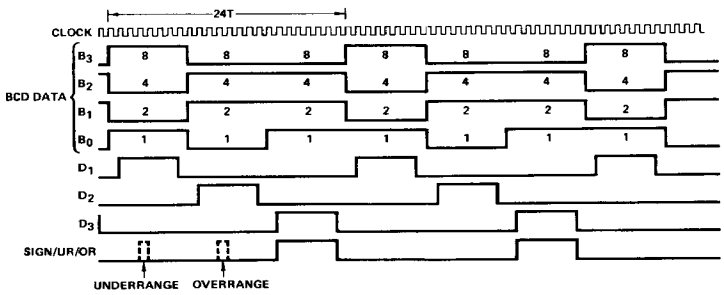
The BCD data stored in the latches is continuously scanned every 24 clock periods (8 clock times per digit). Sign information appears at the SIGN/UR/OR pin coincident with the D_3 strobe. Interdigit blanking of the Digit Strobes is achieved by taking one full clock period from both the leading and trailing edges of the strobes. Thus the digit is on 6 clock periods while the BCD data for that digit appears for the full eight clock periods. Figure 4 shows the Data Output Timing.



Auto-Zero Timing
Figure 2



Measure Interval Timing
Figure 3



Data Output Format
(Output = 769)
Figure 4

APPLICATIONS

1. **Operation Over the Full Frequency Range.** Any sampling rate from 1 to 60 samples per second can be accommodated by simply changing the Integrator and Oscillator Capacitors (C_{INT} and C_{osc}). The Auto-Zero Capacitor (C_{AZ}) should remain at 0.1 μF over the full sampling range.

   a. To find the proper value for C_{osc} refer to the clock frequency Vs. C_{osc} curve shown in the Typical Characteristics. The oscillator frequency and sampling rates are related by:

   $$\text{Sampling Rate} = \frac{f_{osc}}{6144}$$

   b. The integrator capacitor must change as a function of frequency by means of the following relationship:

   $$C_{INT} \cong \frac{1000}{f_{osc}} \ \mu\text{F/sec}$$

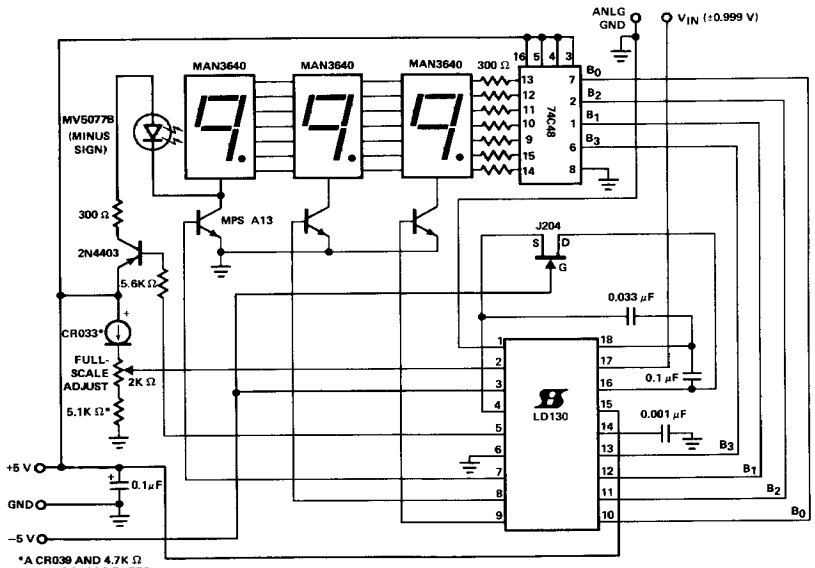
   Capacitor tolerance or type is not critical. C_{AZ} and C_{INT} should have a high insulation resistance over temperature (all film capacitors are suitable).

2. **Supply Voltages.** Minimum supply voltages for operation are V_1 = 4.5 V, V_2 = −4.5 V. Although the LD130 will be functional at these voltages, TTL compatibility can no longer be guaranteed. Maximum voltages for functionality are V_1 = 8 V, V_2 = −8 V. It is recommended that a 0.1 μF or larger capacitor be used to bypass V_1 to ground at the LD130 when LED displays are used.

3. **Reference Voltage.** The typical LD130 application (Figure 5) shows the reference voltage being developed by a current regulator diode-resistor combination. This is the preferred method for creating stable low-voltage references. The temperature compensated current regulator diode (the electrical dual of the temperature compensated Zener) keeps a constant current through the series connection of metal film resistor and cermet trimmer. A typical temperature coefficient of 100 ppM/°C is achieved by this system — an order of magnitude improvement over a typical low-voltage Zener (1N746, 3.3 V Zener).

4. **Input Protection.** The LD130 has protection circuitry at all inputs and outputs which prevent static damage by clamping the voltage at these pins. In many applications, such as a DMM/DVM, the V_{IN} or V_{REF} input may have a high voltage source connected which is capable of supplying destructive currents into the LD130. To prevent such an occurrence, a current limiting resistor should be placed in series with the appropriate input pin. The 1 mA maximum current rating should be observed. A 1M Ω resistor in series with pin 17 of the LD130 would offer input protection up to a 1000 V overvoltage.

5. **Lock-Up Protection.** The E204 J-FET shown in the typical LD130 application of Figure 5 eliminates a power-on lock-up mode. This condition manifests itself by a constant 007 output. If the J-FET is not used, it may be necessary to recycle the power supplies to attain normal operation. The use of the E204 J-FET reduces the maximum allowable negative supply voltage, V_2 to −5.5 V.



3 Digit DVM (±999 mV, 5 samples/sec)
Figure 5

APPLICATIONS (Cont'd)

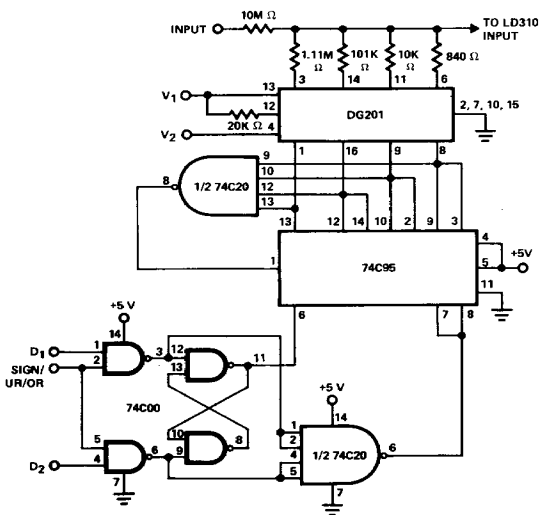
6. **TTL Compatibility.** While both the Digit Strobe (D_1, D_2, D_3) and Data Bit (B_0, B_1, B_2, B_3) outputs are capable of driving 1 TTL load, the maximum internal clock stability, and thus A/D stability, is attained when the bit outputs sink less than 400 μA. Therefore, CMOS or low-power Schottky TTL decoders are preferred. Standard TTL loads will not contribute to A/D instability when an external oscillator is used.

7. **Range Signal Decoding – Autoranging.** The ranging signals (overrange and underrange) are time multiplexed on the SIGN/UR/OR output. De-multiplexing consists of logically ANDING this output with either the D_1 or D_2 Digit Strobe output (see Figure 4). Thus:

   $D_1 \cdot$ SIGN/UR/OR = Underrange Pulse (active high) when count < 80

   $D_2 \cdot$ SIGN/UR/OR = Overrange Pulse (active high) when count > 999

   If either an underrange or overrange condition exists, the appropriate pulse will occur once each sampling interval during the zeroing time. This single pulse can be used directly to step on Autoranging circuit into the next range. Figure 6 shows the implementation of an Autoranging System for the LD130.



Autoranging System For LD130
Figure 6

8. **Ratio operation.** The high impedance reference buffer amplifier and input buffer amplifier make the LD130 very useful in ratio measurements. The ratio error curve shown in the Typical Characteristics section illustrates the A/D transfer function.

$$\text{Count} = \frac{V_{IN}}{V_{REF}} \quad \frac{R_1}{R_2} \; 4096$$

Assuming the ideal design values for R_1 and R_2 (10K Ω and 20.48K Ω) the A/D transfer equation is:

$$\text{Count} = \frac{V_{IN}}{V_{REF}} \times 2000$$

Actual R_1 and R_2 matching tolerance can deviate by 3%.

9. **Inter-Digit Blanking.**

   a. The interdigit blanking period allows the LD130 to interface with gas discharge displays when oscillator frequencies of 16 kHz or less are used.

   b. Since the BCD data for each digit appears before and does not change until after the digit strobe (except when new data is loaded), interface problems such as latching of improper codes are minimized.

   c. The net digit duty cycle is reduced to 25% by the inter-digit blanking period. Average LED currents must be calculated with this consideration.

$$I_{AVg}\ (\text{LED}) = I_{peak} \times 0.25$$

   d. Since the total inter-digit blanking time is equal to a digit ON time, it may be used as a fourth digit strobe for special applications.

10. **High Temperature Operation of the LD130BP**

   a. Device Protection

   The LD130 does have the parasitic SCR structures common to all junction isolated CMOS devices. However, the LD130 includes special protection circuits at both inputs and outputs to minimize the possibility of turning on one of these SCR devices which could lead to excessive power supply drain current and possible device destruction. This possibility, while remote at normal ambient temperatures, is enhanced by operation above 85°C. A 100 Ω resistor in series with the V_1 input of the LD130 will prevent such an occurence at high temperatures while allowing for normal A/D action.

   b. C_{INT}, C_{AZ} Selection

   High temperature operation makes special demands on capacitor values and types. Polycarbonate capacitors are required for C_{INT} and C_{AZ} due to leakage limitations. Although the value of C_{INT} is chosen as

APPLICATIONS (Cont'd)

in paragraph 1, C_{AZ} must be 10 times the value of C_{INT}. This fixes the AZ system damping factor at 0.6 (see AZ equations) and maintains the maximum value of C_{AZ} consistent with proper AZ loop settling.

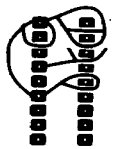
c. Leakage Protection – Pin Guarding

Proper high temperature performance requires that all high impedance inputs (V_{IN}, V_{REF}, AZ) be guarded to minimize pin-to-pin leakage. Good guarding requires a 2 sided glass-epoxy P.C. board with all guard traces and rings driven from low impedance sources. These sources should have a potential close to that of the guarded pin. The board layout of Figure 7 shows the proper method of guarding the inputs of the LD130.

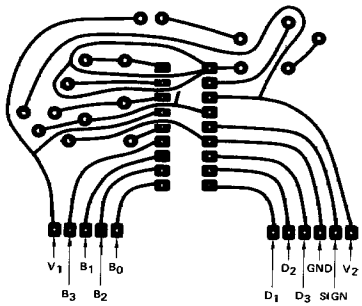
LD130 AZ EQUATIONS

$$\omega_n = \sqrt{\frac{1.25 \times 10^{-9}}{C_{INT}C_{AZ}}}$$

$$\zeta = \sqrt{\frac{1}{32}\left(1 + \frac{C_{INT}}{C_{AZ}} + \frac{C_{AZ}}{C_{INT}}\right)}$$



a.) Top



b.) Bottom

High Temperature PC Board Layout
Figure 7

(refer to Index 6 for 1:1 P.C. patterns)