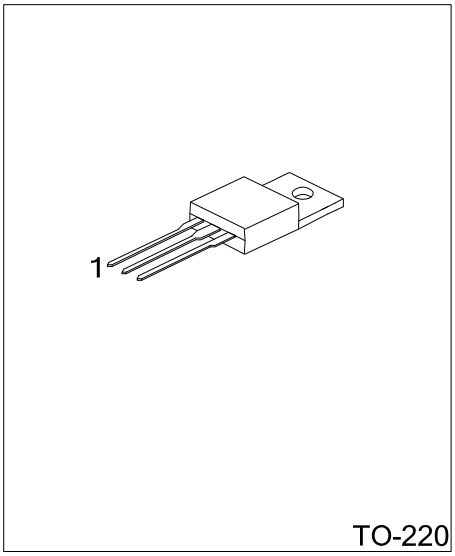
N-CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTOR



■ DESCRIPTION

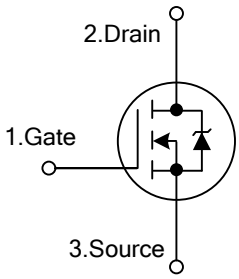
The UTC **25N06** is an N-channel enhancement mode Power MOSFET, which provides low gate charge, avalanche rugged technology, and so on.

The UTC **25N06** is universally applied in DC-DC & DC-AC converters, motor control, high current, high speed switching, solenoid and relay drivers, regulators, audio amplifiers, automotive environment.

■ FEATURES

* Low Gate Charge
* $R_{DS(on)}$ = 0.048 Ω (TYP.)
* Avalanche Rugged Technology
* 100% Avalanche Tested
* Repetitive Avalanche at 100°C
* High Current Capability
* Operating Temperature: 175°C
* Application Oriented Characterization

■ SYMBOL



■ ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
25N06L-TA3-T	25N06G-TA3-T	TO-220	G	D	S	Tube

Note: G: Gate, D: Drain, S: Source

25N06G-TA3-T (1)Packing Type (2)Package Type (3)Halogen Free	(1) T: Tube (2) TA3: TO-220 (3) G: Halogen Free

■ ABSOLUTE MAXIMUM RATINGS

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage (V_{GS}=0)		V_{DS}	60	V
Drain-Gate Voltage (R_{GS}=20kΩ)		V_{DGR}	60	V
Gate-Source Voltage		V_{GS}	± 20	V
Drain Current (Continuous)	T_C=25°C	I_D	25	A
	T_C=100°C		17	A
Drain Current (Pulsed) (Note 2)		I_{DM}	100	A
Single Pulse Avalanche Energy (starting T_J =25°C, I_D =25A, V_{DD} =25 V)		E_{AS}	100	mJ
Total Dissipation at T_C=25°C		P_D	90	W
Maximum Operating Junction Temperature		T_J	175	°C
Storage Temperature		T_{STG}	-65 ~ +175	°C

Note: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.
2. Pulse width limited by safe operating area

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	θ_{JA}	62.5	°C/W
Junction to Case	θ_{JC}	1.57	°C/W

■ ELECTRICAL CHARACTERISTICS (T_C =25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV_{DSS}	I_D=250μA, V_{GS}=0V	60			V
Drain-Source Leakage Current (V_{GS}=0)	I_{DSS}	V_{DS}=Max Rating			1	μA
		V_{DS}= Max Rating×0.8, T_C=125°C			10	
Gate- Source Leakage Current (V_{DS}=0)	I_{GSS}	V_{GS}=±20V			±100	nA
ON CHARACTERISTICS						
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS}=V_{GS}, I_D=250μA	2	2.9	4	V
Static Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=12.5A		0.048	0.065	Ω
On State Drain Current	$I_{D(on)}$	V_{DS}>$I_{D(on)}$ ×$R_{DS(on)max}$, V_{GS}=10V	25			A
Forward Transconductance (Note 1)	g_{FS}	V_{DS}>$I_{D(on)}$ ×$R_{DS(on)max}$, I_D=12.5A	7	11		S
DYNAMIC PARAMETERS						
Input Capacitance	C_{ISS}	V_{GS}=0V, V_{DS}=25V, f=1MHz		700	900	pF
Output Capacitance	C_{OSS}			320	450	pF
Reverse Transfer Capacitance	C_{RSS}			90	150	pF
SWITCHING PARAMETERS						
Total Gate Charge	Q_G	V_{DD}=40V, V_{GS}=10V, I_D=25A		26	40	nC
Gate to Source Charge	Q_{GS}			8		nC
Gate to Drain Charge	Q_{GD}			9		nC
Turn-ON Delay Time	$t_{D(ON)}$	V_{DD}=30V, I_D=3A, R_G=50Ω, V_{GS}=10V		30	45	ns
Rise Time	t_R			90	130	ns
Turn-OFF Delay Time	$t_{D(OFF)}$	V_{DD}=40V, I_D=25A, R_G=50Ω, V_{GS}=10V		80	120	ns
Fall-Time	t_F			80	120	ns
Cross-Over Time	t_C			170	250	ns
Turn-on Current Slope	$(di/dt)_{on}$	V_{DD}=40V, I_D=25A, R_G=50Ω, V_{GS}=10V		230		A/μs
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS						
Drain-Source Diode Forward Voltage (Note 1)	V_{SD}	I_{SD}=25A, V_{GS}=0V			1.5	V
Reverse Recovery Time	t_{RR}	I_{SD}=25A, di/dt=100A/μs, V_{DD}=30V, T_J=150°C		80		ns
Reverse Recovery Charge	Q_{RR}			0.22		μC
Reverse Recovery Current	I_{RRM}			5.5		A
Source-Drain Current	I_{SD}				25	A
Source-Drain Current (Pulsed) (Note 2)	I_{SDM}				100	A

Note: 1. Pulsed: Pulse duration = 300μs, duty cycle 1.5%.
2. Pulse width limited by safe operating area

■ SWITCHING TIME TEST CIRCUIT

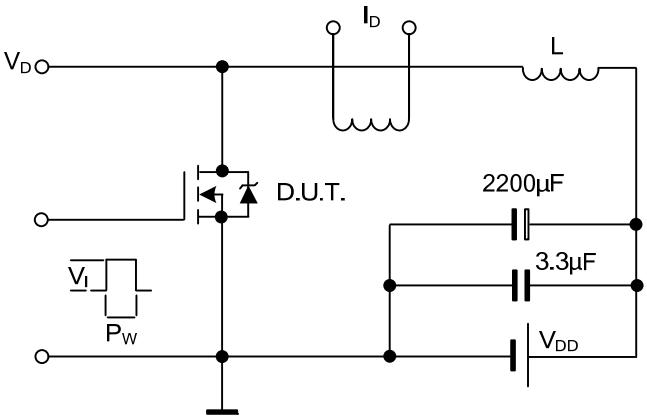


Fig. 1 Unclamped Inductive Load Test Circuits

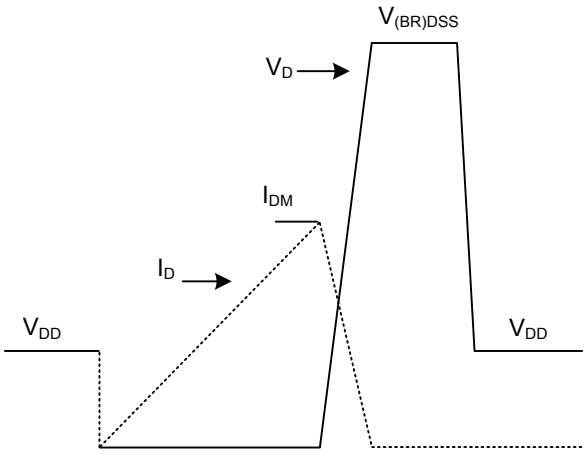


Fig. 2 Unclamped Inductive Waveforms

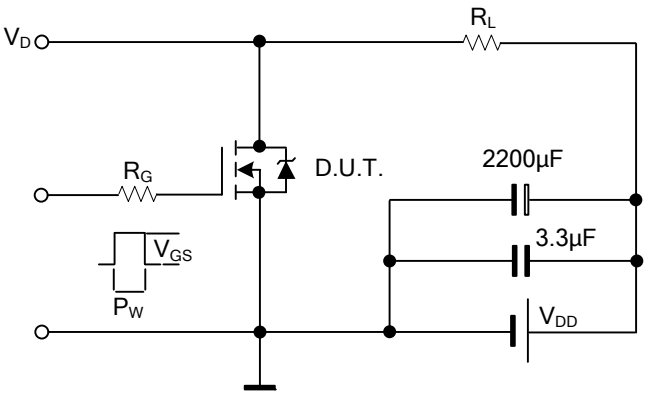


Fig. 3. Switching Times Test Circuits For Resistive Load

■ SWITCHING TIME TEST CIRCUIT (Cont.)

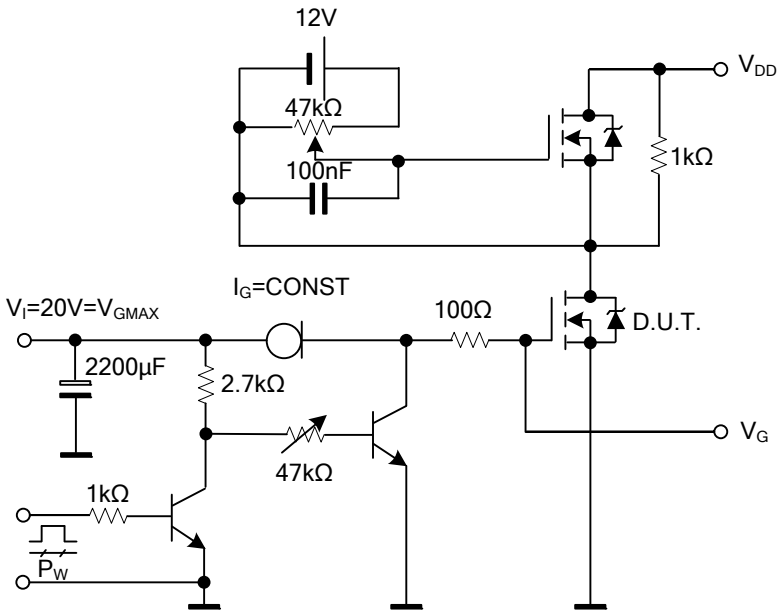


Fig. 4 Gate Charge Test Circuit

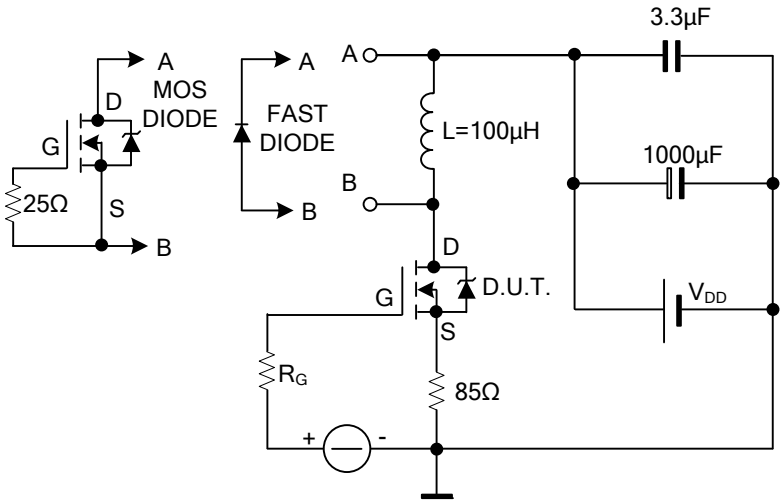


Fig. 5 Test Circuit For Inductive Load Switching And Diode Reverse Recovery Time