EM78P159N

8-Bit Microcontroller with OTP ROM

Product Specification

DOC. VERSION 1.0

ELAN MICROELECTRONICS CORP.

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ELAN MICROELECTRONICS CORPORATION

Contents

APPENDIX

Specification Revision History

Doc. Version	Revision Description	Date
1.0	Initial Release Version	2006/03/10

1 General Description

EM78P159N is an 8-bit microprocessor designed and developed with low-power, high-speed CMOS technology. It is equipped with 1K*13-bits Electrical One Time Programmable Read Only Memory (OTP-ROM). It provides three PROTECTION bits to prevent user's code in the OTP memory from being intruded. 8 OPTION bits are also available to meet user's requirements.

With its OTP-ROM feature, the EM78P159N is able to offer a convenient way of developing and verifying user's programs. Moreover, user can take advantage of ELAN Writer to easily program his development code.

1.1 Comparison between EM78P159N, EM78P154N, and EM78P157N

To find out what similarities and differences are between EM78P159N EM78P154N and EM78P157N, click the following link.

AN-001   EM78P154N/159N introduction and comparison with EM78P157N

2 Features

■ Operating voltage range**:**
  ● 2.1V~5.5V at 0°C~70°C
  ● 2.3V~5.5V at 40°C~85°C

■ Operating frequency range (base on 2 clocks)**:**
  ● Crystal mode**:** DC~20MHz at 5.0V, DC~8MHz at 3.0, DC~4MHz at 2.1V
  ● ERC mode**:**   DC~4MHz at 5.0~2.1V
  ● IRC mode**:**   4 choices of frequencies available; i.e., 8M, 4M, 1M, & 455kHz

■ IRC mode**:**
  ● All these four main frequencies can be trimmed by programming with four calibrated bits in the ICE159N Simulator. OTP is auto trimmed by DWTR.
  ● Temperature, Voltage, and Process changes will influence the frequency drift
  ● Frequency deviation is only ±4.5% after auto trimming (based on Vdd=5V, Ta=25°C)

■ Fast set-up time only requires about 2ms in high XTAL and 32CLKS in IRC mode from wake up to operating mode

■ Low power consumption**:**

- Less then 2mA at 5V/4MHz

- Typically 20μA at 3V/32kHz

- Typically 1μA during Sleep mode

■ 1K $\times$ 13 bits on chip ROM

■ One security register to prevent intrusion of OTP memory codes

■ One configuration register to accommodate user's requirements

■ 48$\times$ 8 bits on chip registers (SRAM, general purpose register)

■ 2 bi-directional I/O ports

■ 5 level stacks for subroutine nesting

■ 8-bit real time clock/counter (TCC) with selective signal sources, trigger edges, and overflow interrupt

■ Two clocks per instruction cycle

■ Power down (SLEEP) mode

■ Three available interruptions**:**

- TCC overflow interrupt

- Input-port status changed interrupt (wake up from Sleep mode)

- External interrupt

■ Programmable free running watchdog timer

■ 8 programmable pull-high pins

■ 8 programmable pull-down pins

■ 8 programmable open-drain pins

■ 2 programmable R-option pins

■ Package types**:**

- 18 pin DIP 300mil   **:** EM78P159NP

- 18 pin SOP 300mil   **:** EM78P159NM

- 20 pin SSOP 209mil **:** EM78P159NAS

- 20 pin SSOP 209mil **:** EM78P159NKM

■ 99.9% single instruction cycle commands

■ The transient point of system frequency between HXT and LXT is around 400kHz

3 Pin Assignments and Descriptions
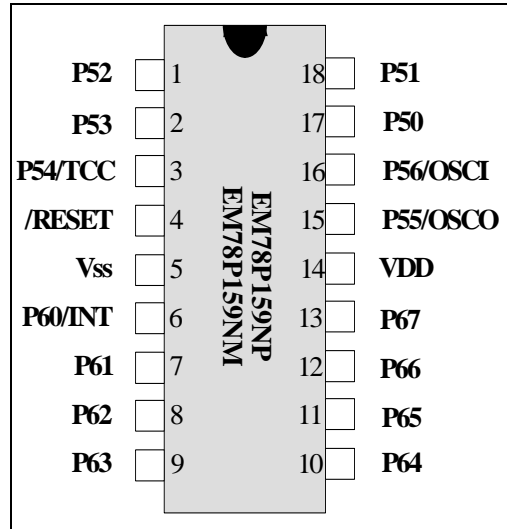
Figure3-1a EM78P159NP/M Pin Assignments
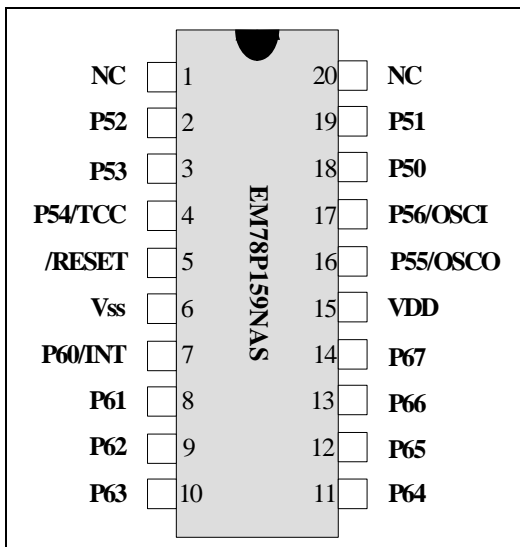
Figure3-1b EM78P159NAS Pin Assignments
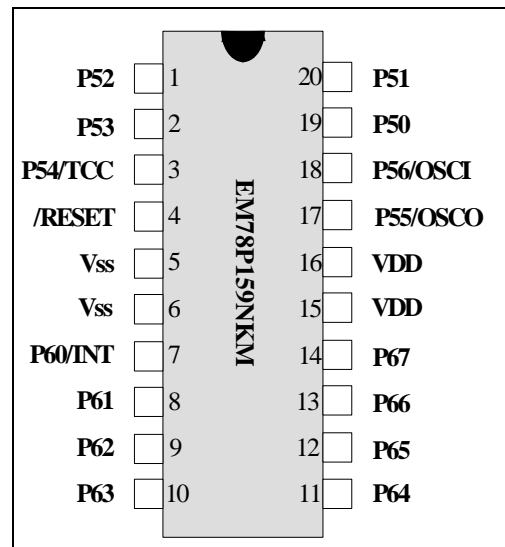
Figure3-1c EM78P159NKM Pin Assignments

3.1 EM78P159NP and EM78P159NM Pin Description

Symbol	Pin No.	Type	Function
VDD	14	-	■ Power supply
P56/OSCI	16	I/O	■ General-purpose I/O pin ■ XTAL type**:** Crystal input terminal or external clock input pin ■ ERC type**:** RC oscillator input pin
P55/OSCO	15	I/O	■ General-purpose I/O pin ■ XTAL type**:** Output terminal for crystal oscillator or external clock input pin ■ RC type**:** Instruction clock output ■ External clock signal input
P54/TCC	3	I/O	■ General-purpose I/O pin ■ The real time clock/counter (with Schmitt trigger input pin), must be tied to VDD or VSS if not in use.
/RESET	4	I	■ Input pin with Schmitt trigger. If this pin remains at logic low, the controller will also remain in reset condition.
P50 ~ P53	17, 18, 1, 2	I/O	■ P50 ~ P53 are bi-directional I/O pins. ■ P50 and P51 can also be defined as the R-option pins ■ P50 ~ P53 can be pulled-down by software
P60 ~ P67	6 ~ 13	I/O	■ P60 ~ P67 are bi-directional I/O pins. ■ These can be pulled-high or can be open-drain by software programming ■ P60 ~ P63 can also be pulled-down by software
/INT	6	I	■ External interrupt pin triggered by falling edge
VSS	5	-	■ Ground

3-2 EM78P159NAS Pin Description

Symbol	Pin No.	Type	Function
VDD	15	-	■ Power supply.
P56/OSCI	17	I/O	■ General-purpose I/O pin ■ XTAL type**:** Crystal input terminal or external clock input pin ■ ERC type**:** RC oscillator input pin
P55/OSCO	16	I/O	■ General-purpose I/O pin ■ XTAL type**:** Output terminal for crystal oscillator or external clock input pin ■ RC type**:** Instruction clock output ■ External clock signal input
P54/TCC	4	I/O	■ General-purpose I/O pin ■ The real time clock/counter (with Schmitt trigger input pin), must be tied to VDD or VSS if not in use.
/RESET	5	I	■ Input pin with Schmitt trigger. If this pin remains at logic low, the controller will also remain in reset condition.
P50~P53	18, 19, 2, 3	I/O	■ P50 ~ P53 are bi-directional I/O pins ■ P50 and P51 can also be defined as the R-option pins ■ P50 ~ P53 can be pulled-down by software
P60~P67	7~14	I/O	■ P60 ~ P67 are bi-directional I/O pins. ■ These can be pulled-high or can be open-drain by software programming ■ P60 ~ P63 can also be pulled-down by software
/INT	7	I	■ External interrupt pin triggered by falling edge
VSS	6	-	■ Ground

3.3　EM78P159NKM Pin Description

Symbol	Pin No.	Type	Function
VDD	15,16	-	■ Power supply.
P56/OSCI	18	I/O	■ General-purpose I/O pin ■ XTAL type: Crystal input terminal or external clock input pin. ■ ERC type: RC oscillator input pin.
P55/OSCO	17	I/O	■ General-purpose I/O pin ■ XTAL type: Output terminal for crystal oscillator or external clock input pin ■ RC type: Instruction clock output ■ External clock signal input
P54/TCC	3	I/O	■ General-purpose I/O pin ■ The real time clock/counter (with Schmitt trigger input pin), must be tied to VDD or VSS if not in use.
/RESET	4	I	■ Input pin with Schmitt trigger. If this pin remains at logic low, the controller will also remain in reset condition.
P50~P53	19, 20, 1, 2	I/O	■ P50 ~ P53 are bi-directional I/O pins. ■ P50 and P51 can also be defined as the R-option pins. ■ P50 ~ P53 can be pulled-down by software.
P60~P67	7~14	I/O	■ P60 ~ P67 are bi-directional I/O pins. ■ These can be pulled-high or can be open-drain by software programming. ■ P60 ~ P63 can also be pulled-down by software
/INT	7	I	■ External interrupt pin triggered by falling edge
VSS	5, 6	-	■ Ground

4   Function Description
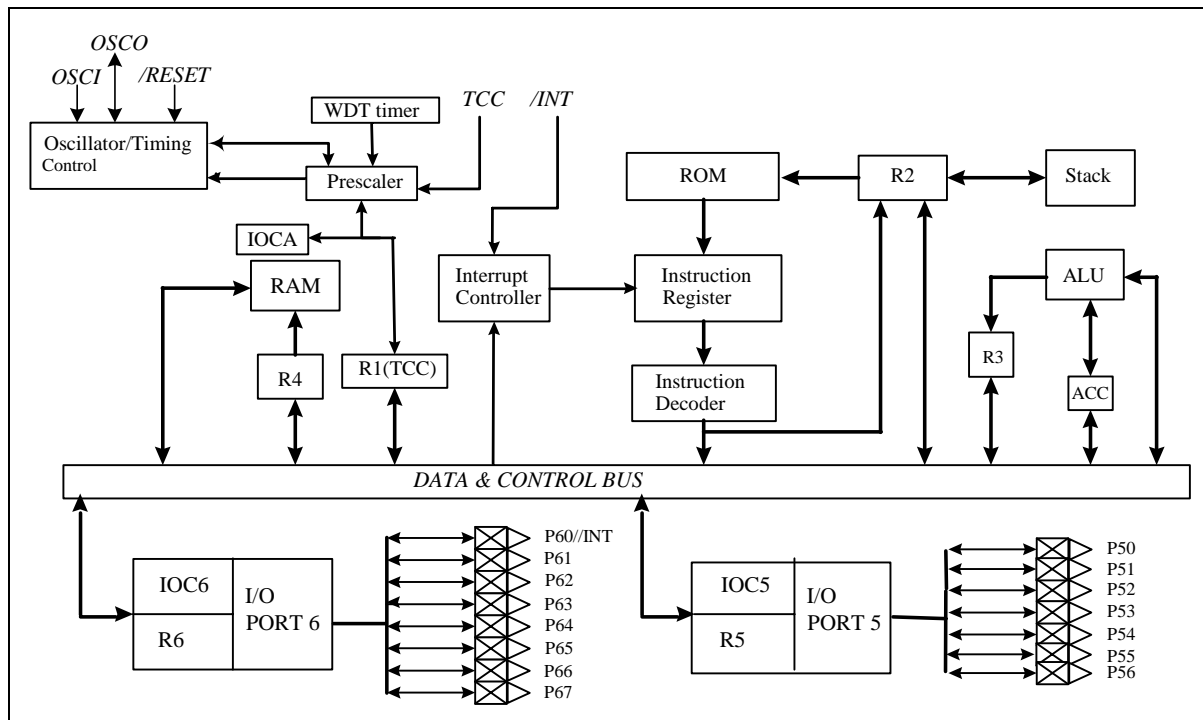
Figure 4-1 Function Block Diagram

4.1   Operational Registers

4.1.1 R0 (Indirect Addressing Register)

R0 is not a physically implemented register. Its major function is to perform as an indirect addressing pointer. Any instruction using R0 as a pointer actually accesses data pointed by the RAM Select Register (R4).

4.1.2 R1 (Time Clock /Counter)

■   Increased by an external signal edge, which is defined by TE bit (CONT-4) through the TCC pin, or by the instruction cycle clock.

■   Writable and readable as any other registers.

■   Defined by resetting PAB(CONT-3).

■   The prescaler is assigned to TCC, if the PAB bit (CONT-3) is reset.

■   The contents of the prescaler counter will be cleared only when TCC register is written with a value.

4.1.3 R2 (Program Counter) & Stack

■   Depending on the device type, R2 and hardware stack are 10-bit wide. The structure is depicted in the following figure.
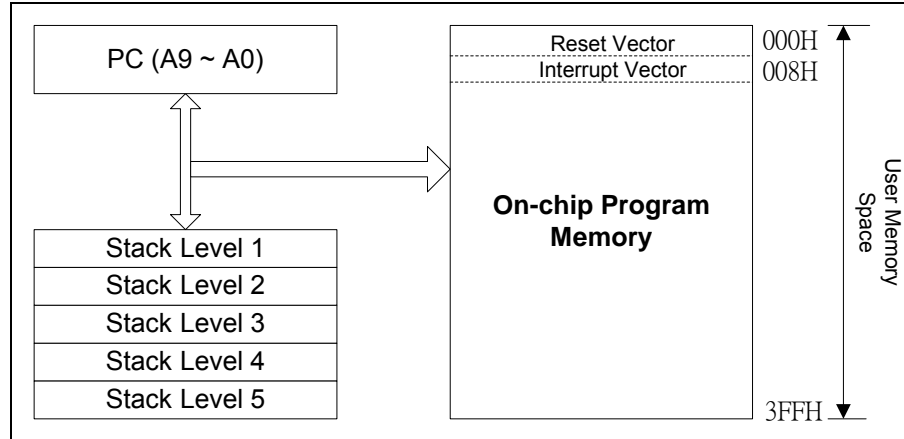
Figure 4-2 Program Counter Organization

■   Generating 1024×13 bits on-chip OTP ROM addresses to the relative programming instruction codes. One program page is 1024 words long.

■   R2 is set as all "0" when under RESET condition.

■   "JMP" instruction allows direct loading of the lower 10 program counter bits. Thus, "JMP" allows PC to go to any location within a page.

■   "CALL" instruction loads the lower 10 bits of the PC, and then PC+1 is pushed into the stack. Thus, the subroutine entry address can be located anywhere within a page.

■   "RET" ("RETLk", "RETI") instruction loads the program counter with the contents of the top-level stack.

■   "ADD R2, A" allows a relative address to be added to the current PC, and the ninth and succeeding bits of the PC will increase progressively.

■   "MOV R2, A" allows loading of an address from the "A" register to the lower 8 bits of the PC, and the ninth and tenth bits (A8 ~ A9) of the PC will remain unchanged.

■   Any instruction (except "ADD R2,A") that is written to R2 (e.g., "MOV R2, A", "BC R2, 6",·····) will cause the ninth bit and the tenth bit (A8 ~ A9) of the PC to remain unchanged.

■   All instructions are single instruction cycle (fclk/2 or fclk/4) except for the instruction that would change the contents of R2. Such instruction will need one more instruction cycle.

■ The Data Memory Configuration is as follows:

Address	R PAGE Registers		IOC PAGE Registers	
00	R0	(IAR)	Reserve	
01	R1	(TCC)	CONT	(Control Register)
02	R2	(PC)	Reserve	
03	R3	(Status)	Reserve	
04	R4	(RSR)	Reserve	
05	R5	(Port5)	IOC5	(I/O Port Control Register)
06	R6	(Port6)	IOC6	(I/O Port Control Register)
07	Reserve		Reserve	
08	Reserve		Reserve	
09	Reserve		Reserve	
0A	Reserve		IOCA	(Prescaler Control Register)
0B	Reserve		IOCB	(Pull-down Register)
0C	Reserve		IOCC	(Open-drain Control)
0D	RD	(Only for simulator)	IOCD	(Pull-high Control Register)
0E	RE	(Wake up control)	IOCE	(WDT Control Register)
0F	RF	(Interrupt Status)	IOCF	(Interrupt Mask Register)
10 : 3F	General Registers			

4.1.4 R3 (Status Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
GP2	GP1	GP0	T	P	Z	DC	C

Bit 0 (C) Carry flag

Bit 1 (DC) Auxiliary carry flag

Bit 2 (Z) Zero flag.

Set to "1" if the result of an arithmetic or logic operation is zero.

Bit 3 (P) Power down bit.

Set to "1" during power on or by a "WDTC" command; and reset to "0" by a "SLEP" command.

Bit 4 (T) Time-out bit.

Set to "1" with the "SLEP" and "WDTC" commands, or during power up; and reset to "0" by WDT time-out.

Bit 5 ~7 (GP0 ~ 2) General-purpose read/write bits.

4.1.5 R4 (RAM Select Register)

Bits 0~5 are used to select registers (Address**:** 00~06, 0F~3F) in the indirect addressing mode.

Bits 6~7 Not used (read only). Set these bits to "1" all the time.

The "Z" flag of R3 will set to "1" when the R4 content is equal to "3F." When R4=R4+1, the R4 content will select "R0."

4.1.6 R5 ~ R6 (Port 5 ~ Port 6)

R5 and **R6** are I/O registers. Only the lower 7 bits of R5 are available.

4.1.7 RD (Manual Calibration Register)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EM78P159N	X	X	X	X	X	X	X	X
ICE159N Simulator	-	-	-	-	C3	C2	C1	C0

In EM78P159N: The register does not exist in real chip.

In ICE159N Simulator: C3 ~ C0 are IRC calibration bits in MCIRC mode.

Bit 3 ~ Bit 0 (C3 ~ C0): are the Calibrators of internal RC mode

C3	C2	C1	C0	Cycle Time (ns)	Frequency (MHz)
0	0	0	0	390.6	2.56
0	0	0	1	365.0	2.74
0	0	1	0	342.5	2.92
0	0	1	1	322.6	3.1
0	1	0	0	304.9	3.28
0	1	0	1	289.0	3.46
0	1	1	0	274.7	3.64
0	1	1	1	261.8	3.82
1	1	1	1	250.0	4.00
1	1	1	0	239.2	4.18
1	1	0	1	229.4	4.36
1	1	0	0	220.3	4.54
1	0	1	1	211.9	4.72
1	0	1	0	204.1	4.9
1	0	0	1	196.7	5.08
1	0	0	0	190.1	5.26

> *NOTES:*
>
> *1. Frequency values shown are theoretical and taken from an instance of a high frequency mode. Hence they are shown for reference only. Definite values will depend on the actual process.*
> *2. Similar way of calculation is also applicable to Low Frequency mode.*

Bits 4~7: Not used

4.1.8   RE (Wake Up Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	-	-	ICWE	-

Bits 0:   Not used.

Bit 1 (ICWE): Port 6 input status change wake-up enable bit

        0 = Disable Port 6 input status change wake-up

        1 = Enable Port 6 input status change wake-up

Bits 2 ~ 7:   Not used.

4.1.9   RF (Interrupt Status Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	-	EXIF	ICIF	TCIF

"1" means interrupt request, and "0" means no interrupt occurs.

Bit 0 (TCIF): TCC overflow interrupt flag. Set when TCC overflows. Reset by software.

Bit 1 (ICIF): Port 6 input status change interrupt flag. Set when Port 6 input changes. Reset by software.

Bit 2 (EXIF): External interrupt flag. Set by falling edge on /INT pin. Reset by software.

Bits 3 ~ 7:   Not used.

RF can be cleared by instruction but cannot be set.

IOCF is the interrupt mask register.

NOTE

The result of reading RF is the "logic AND" of RF and IOCF.

4.1.10   R10 ~ R3F

These are all 8-bit general-purpose registers.

4.2 Special Purpose Registers

4.2.1 A (Accumulator)

■ Internal data transfer, or instruction operand holding

■ It cannot be addressed.

4.2.2 CONT (Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	/INT	TS	TE	PSRE	PSR2	PSR1	PSR0

Bit 0 (PSR0) ~ Bit 2 (PSR2): TCC prescaler bits

PSR2	PSR1	PSR0	TCC Rate
0	0	0	1:2
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

Bit 3 (PSRE): Prescaler enable bit for TCC.

0 = prescaler disabled bit, TCC rate is 1:1

1 = prescaler enabled bit, TCC rate is set as Bit2~Bit0

Bit 4 (TE): TCC signal edge

0 = increment if the transition from low to high takes place on TCC pin

1 = increment if the transition from high to low takes place on TCC pin

Bit 5 (TS): TCC signal source

0 = internal instruction cycle clock, P54 is a bi-directional I/O PIN

1 = transition on TCC pin

Bit 6 (/INT): Interrupt enable flag

0 = masked by DISI or hardware interrupt

1 = enabled by ENI/RETI instructions

Bit 7:   Not used.

CONT register is both readable and writable.

4.2.3 IOC5 ~ IOC6 (I/O Port Control Register)

■ "1" put the relative I/O pin into high impedance, while "0" defines the relative I/O pin as output.

■ Only the lower 7 bits of IOC5 can be defined.

■ IOC5 and IOC6 registers are both readable and writable.

4.2.4 IOCA (Prescaler Counter Register)

■ IOCA register is readable.

■ The value of IOCA is equal to the contents of Prescaler counter.

■ Down counter

4.2.5 IOCB (Pull-Down Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
/PD7	/PD6	/PD5	/PD4	/PD3	/PD2	/PD1	/PD0

Bit 0 (/PD0): Control bit is used to enable the pull-down of P50 pin.

> **0** = Enable internal pull-down
>
> **1** = Disable internal pull-down

Bit 1 (/PD1): Control bit is used to enable the pull-down of P51 pin.

Bit 2 (/PD2): Control bit is used to enable the pull-down of P52 pin.

Bit 3 (/PD3): Control bit is used to enable the pull-down of P53 pin.

Bit 4 (/PD4): Control bit is used to enable the pull-down of P60 pin.

Bit 5 (/PD5): Control bit is used to enable the pull-down of P61 pin.

Bit 6 (/PD6): Control bit is used to enable the pull-down of P62 pin.

Bit 7 (/PD7): Control bit is used to enable the pull-down of P63 pin.

IOCB Register is both readable and writable.

4.2.6 IOCC (Open-Drain Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OD7	OD6	OD5	OD4	OD3	OD2	OD1	OD0

Bit 0 (OD0): Control bit is used to enable the open-drain of P60 pin.

> **0** = Disable open-drain output

> **1** = Enable open-drain output

Bit 1 (OD1): Control bit is used to enable the open-drain of P61 pin.

Bit 2 (OD2): Control bit is used to enable the open-drain of P62 pin.

Bit 3 (OD3): Control bit is used to enable the open-drain of P63 pin.

Bit 4 (OD4): Control bit is used to enable the open-drain of P64 pin.

Bit 5 (OD5): Control bit is used to enable the open-drain of P65 pin.

Bit 6 (OD6): Control bit is used to enable the open-drain of P66 pin.

Bit 7 (OD7): Control bit is used to enable the open-drain of P67 pin.

IOCC Register is both readable and writable.

4.2.7 IOCD (Pull-High Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
/PH7	/PH6	/PH5	/PH4	/PH3	/PH2	/PH1	/PH0

Bit 0 (/PH0): Control bit is used to enable the pull-high of P60 pin.

> **0** = Enable internal pull-high

> **1** = Disable internal pull-high

Bit 1 (/PH1): Control bit is used to enable the pull-high of P61 pin.

Bit 2 (/PH2): Control bit is used to enable the pull-high of P62 pin.

Bit 3 (/PH3): Control bit is used to enable the pull-high of P63 pin.

Bit 4 (/PH4): Control bit is used to enable the pull-high of P64 pin.

Bit 5 (/PH5): Control bit is used to enable the pull-high of P65 pin.

Bit 6 (/PH6): Control bit is used to enable the pull-high of P66 pin.

Bit 7 (/PH7): Control bit is used to enable the pull-high of P67 pin.

IOCD Register is both readable and writable.

4.2.8 IOCE (WDT Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WDTE	EIS	-	ROC	PSWE	PSW2	PSW1	PSW0

Bit 7 (WDTE): Control bit used to enable the Watchdog timer.

> **0** = Disable WDT
>
> **1** = Enable WDT
>
> WDTE is both readable and writable.

Bit 6 (EIS): Control bit is used to define the function of P60 (/INT) pin.

> **0** = P60, bi-directional I/O pin.
>
> **1** = /INT, external interrupt pin. In this case, the I/O control bit of P60 (Bit 0 of IOC6) must be set to "1."
>
> When EIS is "0," the path of /INT is masked. When EIS is "1," the status of /INT pin can also be read by way of reading Port 6 (R6). See Figure 4-4a under Section 4.4 for reference.
>
> EIS is both readable and writable.

Bit 5: Not used

Bit 4 (ROC): ROC is used for the R-option.

> Setting the ROC to "1" will enable the status of R-option pins (P50~P51) that are read by the controller. Clearing the ROC will disable the R-option function. If the R-option function is selected, you must connect the P51 pin or/and P50 pin to VSS with a 430KΩ external resistor (Rex). If the Rex is connected/disconnected, the status of P50 (P51) is read as "0" / "1." Refer to Figure 4-5 under Section 4.4 for reference.

Bit 3 (PSWE): Prescaler enable bit for WDT

> **0** = prescaler disable bit, WDT rate is 1**:**1.
>
> **1** = prescaler enable bit, WDT rate is set as Bit4~Bit2.

Bit 2 (PSW2) ~ Bit 0 (PSW0): WDT prescaler bits

PSW2	PSW1	PSW0	WDT Rate
0	0	0	1:2
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

4.2.9 IOCF (Interrupt Mask Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	-	EXIE	ICIE	TCIE

Bit 0 (TCIE): TCIF interrupt enable bit

    0 = disable TCIF interrupt

    1 = enable TCIF interrupt

Bit 1 (ICIE): ICIF interrupt enable bit

    0 = disable ICIF interrupt

    1 = enable ICIF interrupt

Bit 2 (EXIE): EXIF interrupt enable bit

    0 = disable EXIF interrupt

    1 = enable EXIF interrupt

Bits 3~7:   Not used

Individual interrupt is enabled by setting its associated control bit in the IOCF to "1."

Global interrupt is enabled by the ENI instruction and is disabled by the DISI instruction. Refer to Figure 4-7 in Section 4.6 for further reference.

IOCF register is both readable and writable.

4.3 TCC/WDT & Prescaler

There are two 8-bit counters available as prescalers for the TCC and WDT respectively. The PSR0 ~ PSR2 bits of the CONT register are used to determine the ratio of the prescaler of TCC, and the PWR0 ~ PWR2 bits of the IOCE register are used to determine the prescaler of WDT. The prescaler (PSR0 ~ PSR2) will be cleared by the instruction each time it writes to TCC. The WDT and prescaler will be cleared by the "WDTC" and "SLEP" instructions.

■   R1 (TCC) is an 8-bit timer/counter. The clock source of TCC can be internal or external clock input (edge selectable from TCC pin). If TCC signal is sourced from internal clock, TCC will increase by 1 at every instruction cycle (without prescaler). CLK=Fosc/2 or CLK=Fosc/4 application is determined by the CODE Option bit CLK status. CLK=Fosc/2 is used if CLK bit is "0," and CLK=Fosc/4 is used if CLK bit is "1." If TCC signal source comes from external clock input, TCC is increased by 1 at every falling edge or rising edge of TCC pin.

■   The watchdog timer is a free running on-chip RC oscillator. The WDT will keep on running even when the oscillator driver has been turned off (i.e., in Sleep mode). During normal operation or Sleep mode, a WDT time-out (if enabled) will cause the device to reset. The WDT can be enabled or disabled any time during Normal mode by software programming. Refer to WDTE bit of IOCE register in Section 4.2.8. Without prescaler, the WDT time-out period is approximately 18 ms[1] (default).

---

[1] Vdd = 5V, set up time period = 16.8ms ± 30%

    Vdd = 3V, set up time period = 18ms ± 30%

4.4 I/O Ports

The I/O registers, both Port 5 and Port 6, are bi-directional tri-state I/O ports. Port 6 can be pulled high internally by software. In addition, Port 6 can also features an open-drain output through software and an Input status change interrupt (or wake-up) function. P50 ~ P53 and P60 ~ P63 pins can be pulled down by software. Each I/O pin can be defined as "input" or "output" pin by the I/O control register (IOC5 ~ IOC6). P50~P51 are the R-option pins enabled by setting the ROC bit in the IOCE register to "1." When the R-option function is used, it is recommended that P50 ~ P51 are used as output pins. When R-option is in enable state, P50 ~ P51 must be programmed as input pins. Under R-option mode, the current/power consumption by Rex should be taken into the consideration to promote energy conservation.

The I/O registers and I/O control registers are both readable and writable. The I/O interface circuits for Port 5 and Port 6 are shown in the following figures (Figures 4-3, 4-4a, 4-4b, & 4-5).
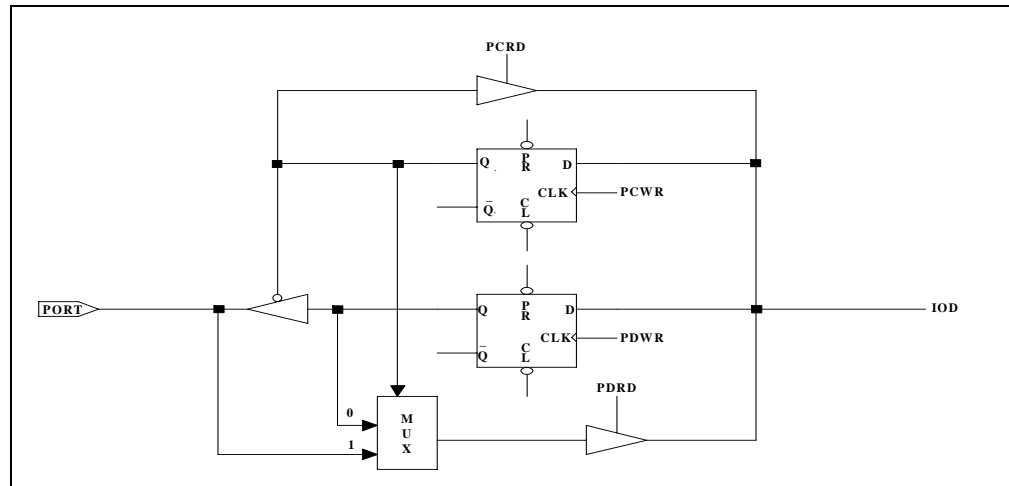
Figure 4-3 I/O Port and I/O Control Register for Port 5 Circuit

NOTE
Pull-down is not shown in the figure.
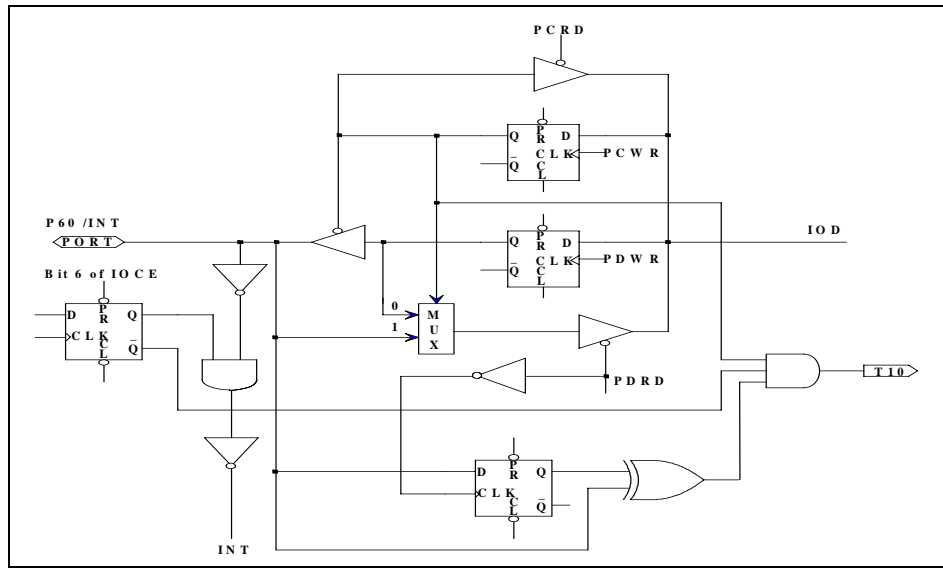
Figure 4-4a I/O Port and I/O Control Register for P60 (/INT) Circuit

NOTE
Pull-high (down) and Open-drain are not shown in the figure.
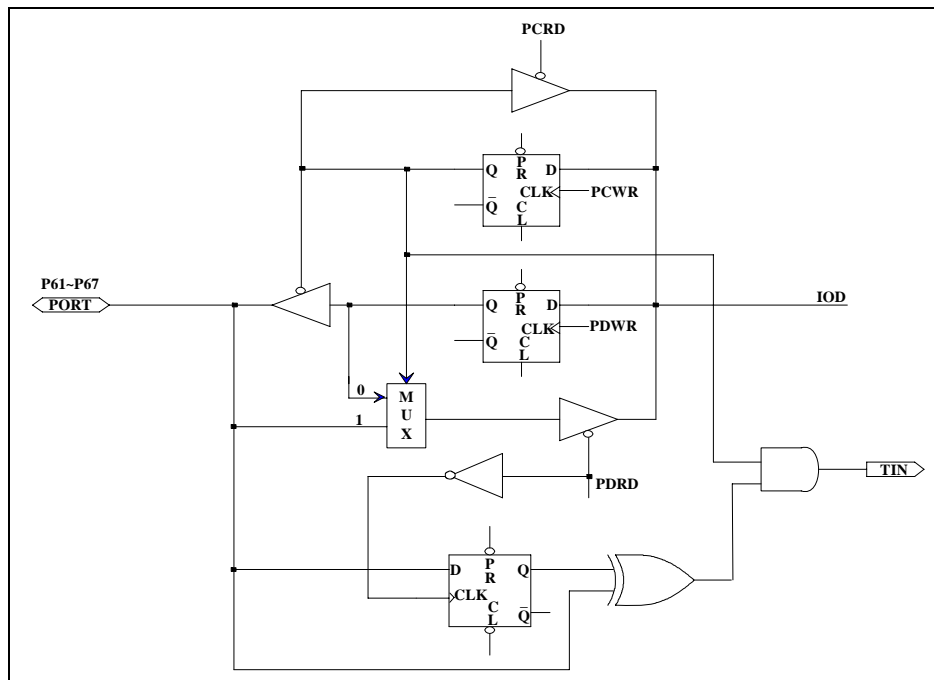
Figure 4-4b I/O Port and I/O Control Register for P61~P67 Circuit

NOTE
Pull-high (down) and Open-drain are not shown in the figure.
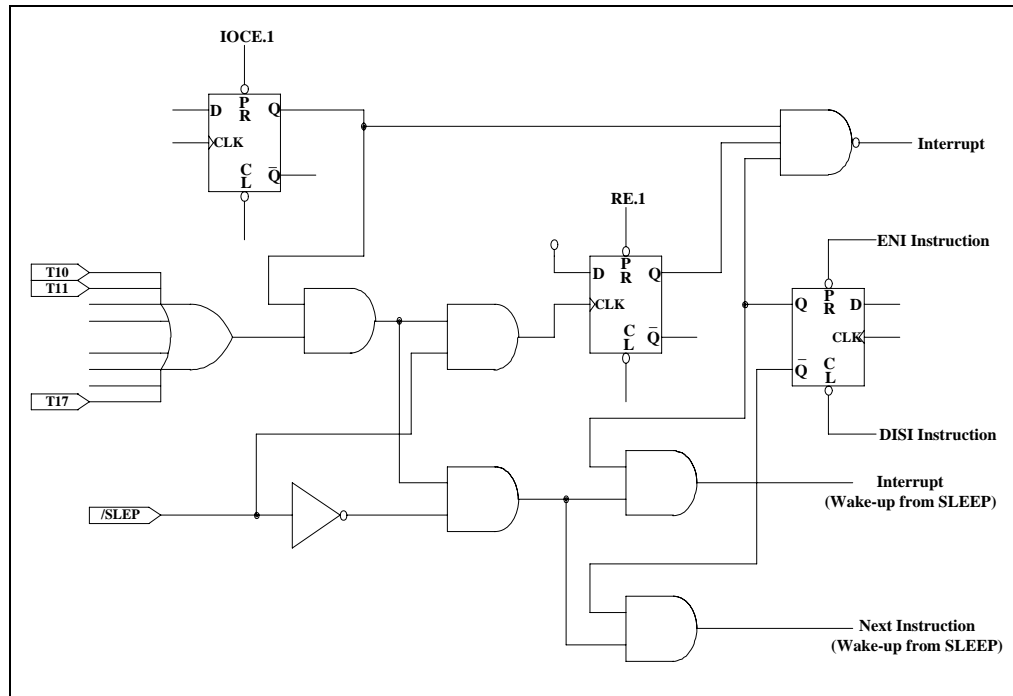
Figure 4-4c I/O Port 6 with Input Change Interrupt/Wake-up Block Diagram

4.4.1 Usage of Port 6 Input Change Wake-up/Interrupt Function

Usage of Port 6 Input Status Changed Wake-up/Interrupt	
(I) Wake-up	(II) Wake-up and interrupt
(a) Before SLEEP	(a) Before SLEEP
1. Disable WDT	1. Disable WDT
2. Read I/O Port 6 (MOV R6,R6)	2. Read I/O Port 6 (MOV R6,R6)
3. Execute "ENI" or "DISI"	3. Execute "ENI" or "DISI"
4. Enable wake-up bit (Set RE ICWE =1)	**4. Enable wake-up bit (Set RE ICWE =1)**
5. Execute "SLEP" instruction	**5. Enable interrupt (Set IOCF ICIE =1)**
(b) After wake-up	6. Execute "SLEP" instruction
→ Next instruction	(b) After wake-up
	1. IF "ENI" → Interrupt vector (008H)
	2. IF "DISI" → Next instruction
(III) Interrupt	
(a) Before Port 6 pin change	
1. Read I/O Port 6 (MOV R6,R6)	
2. Execute "ENI" or "DISI"	
3. Enable interrupt (Set IOCF0 ICIE =1)	
(b) After Port 6 pin changed (interrupt)	
1. IF "ENI" → Interrupt vector (008H)	
2. IF "DISI" → Next instruction	
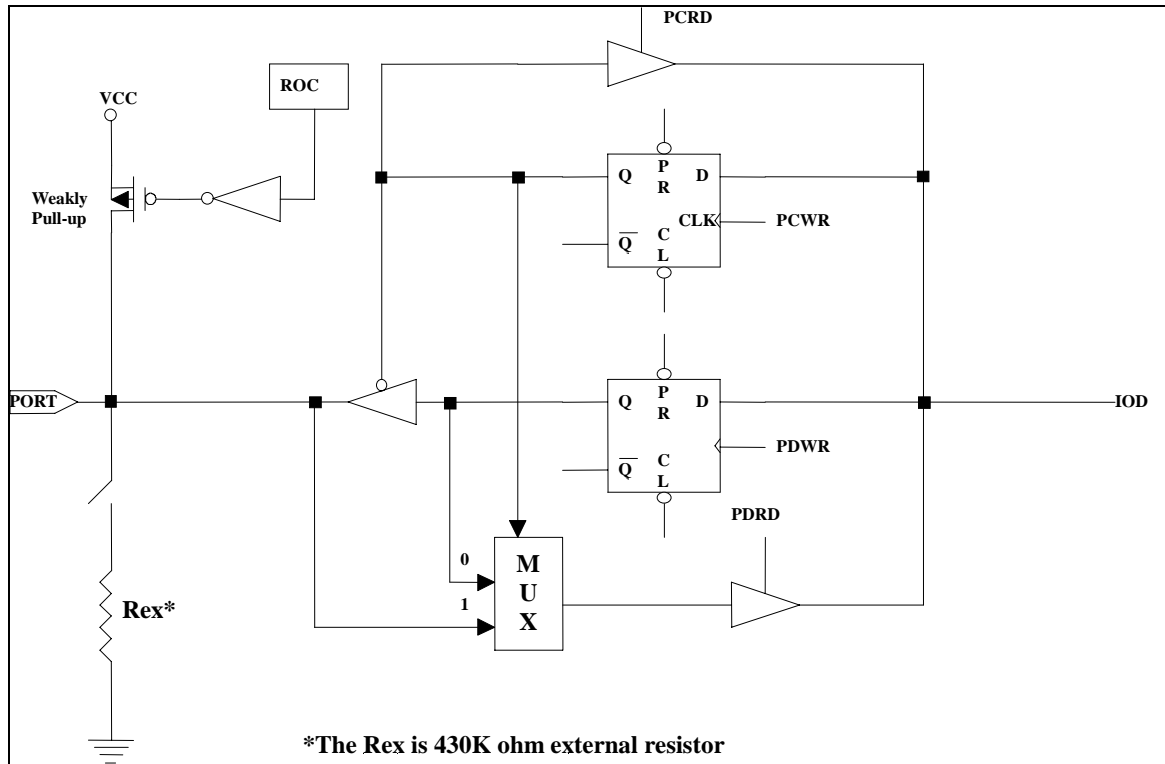
Figure 4-5 I/O Port with R-option (P50,P51) Circuit

4.5 RESET and Wake-up

4.5.1 RESET

A RESET is initiated by one of the following events-

1) Power on reset.

2) /RESET pin input "low," or

3) WDT time-out (if enabled).

The device is kept under RESET condition for a period of approximately 18ms[2] (one oscillator start-up timer period) after a reset is detected. And if the /Reset pin goes "low" or WDT time-out is active, a reset is generated. Once a RESET occurs, the following functions are performed**:**

■ The oscillator is running, or will be started.

■ The Program Counter (R2) is set to all "0."

■ All I/O port pins are configured as input mode (high-impedance state).

---

[2] Vdd = 5V, set up time period = 16.8ms ± 30%
Vdd = 3V, set up time period = 18ms ± 30%

■ The Watchdog timer and prescaler are cleared.

■ When power is switched on, the upper 3 bits of R3 are cleared.

■ The bits of the CONT register are set to all "1" except for the Bit 6 (INT flag).

■ The bits of the IOCA register are set to all "1."

■ The bits of the IOCB register are set to all "1."

■ The IOCC register is cleared.

■ The bits of the IOCD register are set to all "1."

■ Bit 7 of the IOCE register is set to "1," and Bits 4 and 6 are cleared.

■ Bits 0 ~ 2 of RF and Bits 0 ~ 2 of IOCF registers are cleared.

The Sleep (power down) mode is asserted by executing the "SLEP" instruction. While entering Sleep mode, WDT (if enabled) is cleared but keeps on running. The controller can be awakened by-

1) External reset input on /RESET pin,

2) WDT time-out (if enabled), or

3) Port 6 input status change (if enabled).

The first two cases will cause the EM78P159N to reset. The T and P flags of R3 are used to determine the source of the reset (wake-up). The last case is considered the continuation of program execution and the global interrupt ("ENI" or "DISI" being executed) decides whether or not the controller branches to the interrupt vector following wake-up. If ENI is executed before SLEP, the instruction will begin to execute from the address 008H after wake-up. If DISI is executed before SLEP, the operation will restart from the succeeding instruction right next to SLEP after wake-up.

Wake-up time is dependent on oscillator mode. Under RC mode, the reset time is 32 clocks, and in High XTAL mode, reset time is 2ms and 32clocks. In Low XTAL mode, the reset time is 500ms. The above is applicable only for stable oscillator.

Only one of Cases 2 and 3 can be enabled before going into the Sleep mode. That is,

[a] if Port 6 Input Status Change Interrupt is enabled before SLEP, WDT must be disabled by software. However, the WDT bit in the option register remains enabled. Hence, the EM78P159N can be awakened only by Case 1 or 3.

[b] if WDT is enabled before SLEP, Port 6 Input Status Change Interrupt must be disabled. Hence, the EM78P159N can be awakened only by Case 1 or 2. Refer to the Section 4.6, *Interrupt* for further details.

If Port 6 Input Status Change Interrupt is used to wake-up the EM78P159N (Case [a] above), the following instructions must be executed before SLEP:

```
MOV A, @xx000110b     ; Select internal TCC clock

CONTW

CLR R1                ; Clear TCC and prescaler

MOV A, @xxxx1110b     ; Select WDT prescaler

CONTW

WDTC                  ; Clear WDT and prescaler

MOV A, @0xxxxxxxb     ;Disable WDT

IOW RE

MOV R6, R6            ; Read Port 6

BS RE,1               ; Enable wake up control bit

MOV A, @00000x1xb     ; Enable Port 6 input change interrupt

IOW RF

ENI (or DISI)         ; Enable (or disable) global interrupt

SLEP                  ;Sleep

NOP
```

4.5.2 The Summary of the Initialized Values for Registers

Address	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
N/A	IOC5	Bit Name	X	C56	C55	C54	C53	C52	C51	C50
		Power-On	U	1	1	1	1	1	1	1
		/RESET and WDT	U	1	1	1	1	1	1	1
		Wake-Up from Pin Change	U	P	P	P	P	P	P	P
N/A	IOC6	Bit Name	C67	C66	C65	C64	C63	C62	C61	C60
		Power-On	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
N/A	CONT	Bit Name	X	/INT	TS	TE	PSRE	PSR2	PSR1	PSR0
		Power-On	1	0	1	1	1	1	1	1
		/RESET and WDT	1	0	1	1	1	1	1	1
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0x00	R0(IAR)	Bit Name	-	-	-	-	-	-	-	-
		Power-On	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0x01	R1(TCC)	Bit Name	-	-	-	-	-	-	-	-
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0x02	R2(PC)	Bit Name	-	-	-	-	-	-	-	-
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	*0/P	*0/P	*0/P	*0/P	*1/P	*0/P	*0/P	*0/P
0x03	R3(SR)	Bit Name	GP2	GP1	GP0	T	P	Z	DC	C
		Power-On	0	0	0	1	1	U	U	U
		/RESET and WDT	0	0	0	**	**	P	P	P
		Wake-Up from Pin Change	P	P	P	**	**	P	P	P
0x04	R4(RSR)	Bit Name	-	-	-	-	-	-	-	-
		Power-On	1	1	U	U	U	U	U	U
		/RESET and WDT	1	1	P	P	P	P	P	P
		Wake-Up from Pin Change	1	1	P	P	P	P	P	P
0x05	P5	Bit Name	X	P56	P55	P54	P53	P52	P51	P50
		Power-On	0	U	U	U	U	U	U	U
		/RESET and WDT	0	P	P	P	P	P	P	P
		Wake-Up from Pin Change	0	P	P	P	P	P	P	P
0x06	P6	Bit Name	P67	P66	P65	P64	P63	P62	P61	P60
		Power-On	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P

Address	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0E	RE(WUE)	Bit Name	X	X	X	X	X	X	ICWE	X
		Power-On	U	U	U	U	U	U	0	U
		/RESET and WDT	U	U	U	U	U	U	0	U
		Wake-Up from Pin Change	U	U	U	U	U	U	P	U
0x0F	RF(ISR)	Bit Name	X	X	X	X	X	EXIF	ICIF	TCIF
		Power-On	U	U	U	U	U	0	0	0
		/RESET and WDT	U	U	U	U	U	0	0	0
		Wake-Up from Pin Change	U	U	U	U	U	P	P	P
0x0A	IOCA	Bit Name	-	-	-	-	-	-	-	-
		Power-On	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0x0B	IOCB	Bit Name	/PD7	/PD6	/PD5	/PD4	/PD3	/PD2	/PD1	/PD0
		Power-On	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0x0C	IOCC	Bit Name	OD7	OD6	OD5	OD4	OD3	OD2	OD1	OD0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0x0D	IOCD	Bit Name	/PH7	/PH6	/PH5	/PH4	/PH3	/PH2	/PH1	/PH0
		Power-On	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0x0E	IOCE	Bit Name	WDTE	EIS	X	ROC	PSWE	PSW2	PSW1	PSW0
		Power-On	1	0	U	0	0	0	0	0
		/RESET and WDT	1	0	U	0	0	0	0	0
		Wake-Up from Pin Change	1	P	U	P	P	P	P	P
0x0F	IOCF	Bit Name	X	X	X	X	X	EXIE	ICIE	TCIE
		Power-On	U	U	U	U	U	0	0	0
		/RESET and WDT	U	U	U	U	U	0	0	0
		Wake-Up from Pin Change	U	U	U	U	U	P	P	P
0x10~0x2F	R10~R2F	Bit Name	-	-	-	-	-	-	-	-
		Power-On	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P

* J*ump to address 0x08, or execute the instruction next to the "SLEP" instruction.*

** *Refer to tables provided under next section (Section 4.5.3).*

Legend:

X: Not used   **U:** Unknown or don't care   **P:** Previous value before reset

4.5.3 The Status of RST, T, and P of STATUS Register

A RESET condition is initiated by the following events

1) A power-on condition,

2) A high-low-high pulse on /RESET pin, and

3) Watchdog timer time-out.

The values of T and P listed in the table below are used to check how the processor wakes up.

■ **The Values of RST, T, and P after RESET**

Reset Type	T	P
Power on	1	1
/RESET during Operating mode	*P	*P
/RESET wake-up during SLEEP mode	1	0
WDT during Operating mode	0	*P
WDT wake-up during SLEEP mode	0	0
Wake-Up on pin change during SLEEP mode	1	0

* *P: Previous status before reset*

The following table shows the events that may affect the status of T and P.

■ **The Status of T and P Being Affected by Events**

Event	T	P
Power on	1	1
WDTC instruction	1	1
WDT time-out	0	*P
SLEP instruction	1	0
Wake-Up on pin change during SLEEP mode	1	0

* *P: Previous status before reset*
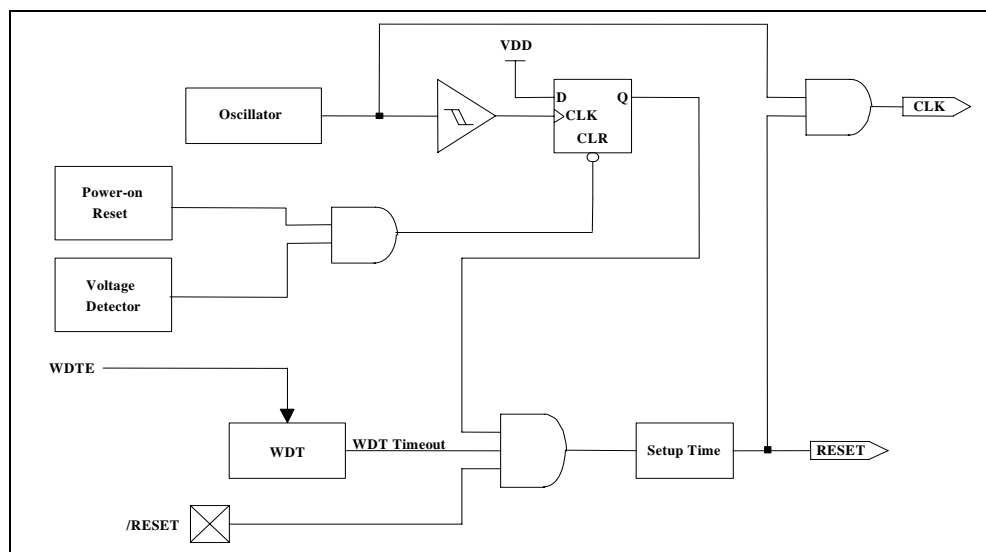
Figure 4-6 Controller Reset Block Diagram

4.6 Interrupt

The EM78P159N has three falling-edge interrupts as listed herewith**:**

1) TCC overflow interrupt

2) Port 6 Input Status Change Interrupt

3) External interrupt [(P60, /INT) pin].

Before the Port 6 Input Status Change Interrupt is enabled, reading Port 6 (e.g., "MOV R6,R6") is necessary. Each Port 6 pin will have this feature if its status changes. Any pin configured as output or P60 pin configured as /INT is excluded from this function. The Port 6 Input Status Changed Interrupt can wake up the EM78P159N from Sleep mode if Port 6 is enabled prior to going into the Sleep mode by executing SLEP. When the chip wakes-up, the controller will continue to execute the succeeding address if the global interrupt is disabled or it will branch into the interrupt vector 008H if the global interrupt is enabled.

RF is the interrupt status register that records the interrupt requests in the relative flags/bits. IOCF is an interrupt mask register. The global interrupt is enabled by the ENI instruction and is disabled by the DISI instruction. When one of the interrupts (enabled) occurs, the next instruction will be fetched from address 008H. Once in the interrupt service routine, the source of an interrupt can be determined by polling the flag bits in RF. The interrupt flag bit must be cleared by instructions before leaving the interrupt service routine and before interrupts are enabled to avoid recursive interrupts.

The flag (except ICIF bit) in the Interrupt Status Register (RF) is set regardless of the status of its mask bit or the execution of ENI. Note that the outcome of RF will be the logic AND of RF and IOCF (refer to figure below). The RETI instruction ends the interrupt routine and enables the global interrupt (the execution of ENI).

When an interrupt is generated by the INT instruction (enabled), the next instruction will be fetched from Address 001H.
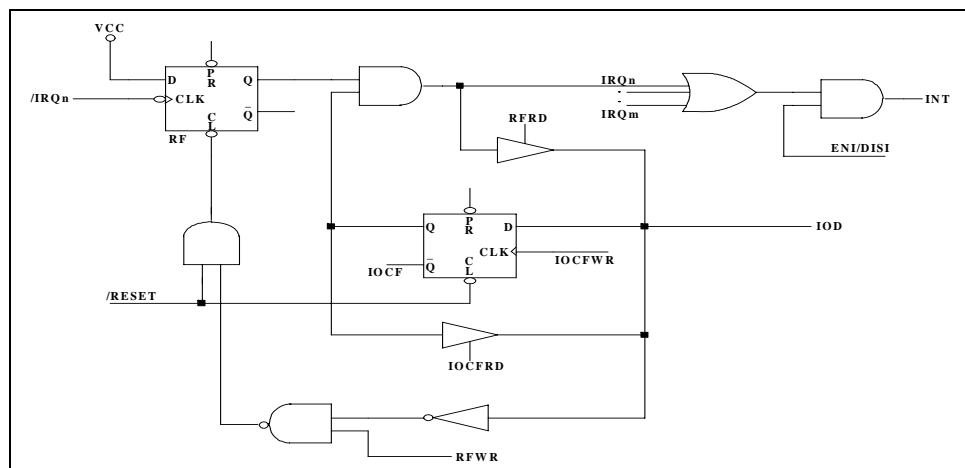
Figure 4-7 Interrupt Input Circuit

4.7 Oscillator

4.7.1 Oscillator Modes

The EM78P159N can be operated in four different oscillator modes, such as External RC oscillator mode (ERC), Internal RC oscillator mode(IRC), High XTAL oscillator mode (HXT), and Low XTAL oscillator mode (LXT). The desired mode can be selected through programming of OSC2, OSC1, and OSC0 in the CODE option register. Table below explains how these 4 oscillator modes are defined with OSC2, OSC1, and OSC0.

■ **Oscillator Modes Defined by OSC**

Mode		OSC2	OSC1	OSC0
ERC (External RC oscillator mode); P55/OSCO act P55		0	0	0
ERC (External RC oscillator mode); P55/OSCO act OSCO		0	0	1
IRC (Internal RC oscillator mode) ; P55/OSCO act P55		0	1	0
IRC (Internal RC oscillator mode); P55/OSCO act OSCO		0	1	1
MCIRC (Manual calibration IRC mode); P55/OSCO act P55	With Simulator only	1	0	0
MCIRC (Manual calibration IRC mode); P55/OSCO act OSCO		1	0	1
LXT (Low XTAL oscillator mode)		1	1	0
HXT (High XTAL oscillator mode) **(default)**		1	1	1

NOTE
The transient point of system frequency between HXT and LXY is around 400 KHz.

The maximum operational frequency of crystal/resonator under different VDDs is as listed below.

■ **Summary of Maximum Operating Speeds**

Conditions	VDD	Max Freq. (MHz)
Two cycles with two clocks	2.1	4.0
	3.0	8.0
	5.0	20.0

4.7.2 *Crystal Oscillator/Ceramic Resonators (XTAL)*

EM78P159N can be driven by an external clock signal through the OSCI pin as shown in the following figure.
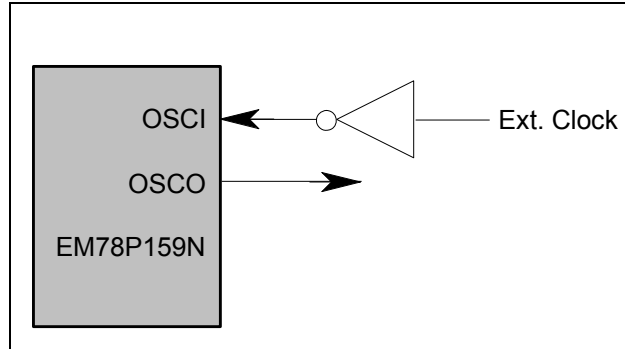
Figure 4-8a External Clock Input Circuit

In the most applications, Pin OSCI and Pin OSCO can be connected with a crystal or ceramic resonator to generate oscillation. Figure below depicts such circuit. The same thing applies whether it is in the HXT mode or in the LXT mode. The following table provides the recommended values of C1 and C2. Since each resonator has its own attribute, you should refer to its specification for appropriate values of C1 and C2. RS, a serial resistor, may be necessary for AT strip cut crystal or low frequency mode.
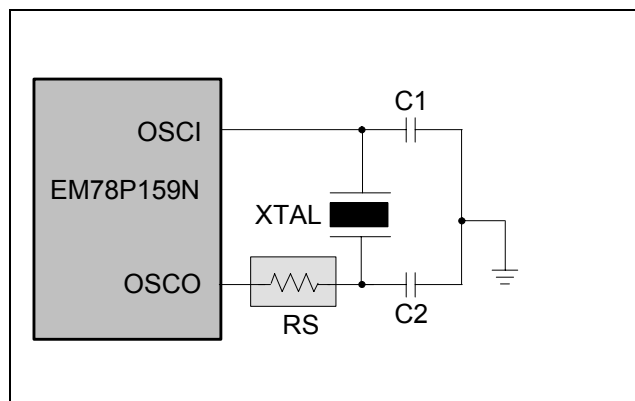
Figure 4-8b Crystal/Resonator Circuit

■   **Capacitor Selection Guide for Crystal Oscillator or Ceramic Resonator**

Oscillator Type	Frequency Mode	Frequency	C1(pF)	C2(pF)
Ceramic Resonators	HXT	455 kHz	100~150	100~150
		2.0 MHz	20~40	20~40
		4.0 MHz	10~30	10~30
Crystal Oscillator	LXT	32.768kHz	25	15
		100KHz	25	25
		200KHz	25	25
	HXT	455KHz	20~40	20~150
		1.0MHz	15~30	15~30
		2.0MHz	15	15
		4.0MHz	15	15

> **NOTE**
> *The values of capacitors C1 & C2 are for reference only.*

4.7.3 External RC Oscillator Mode

For some applications that do not need a very precise timing calculation, the RC oscillator (Figure 4-9 below) offers a lot of cost savings. Nevertheless, it should be noted that the frequency of the RC oscillator is influenced by the supply voltage, the values of the resistor (Rext), the capacitor (Cext), and even by the operation temperature. Moreover, the frequency also changes slightly from one chip to another due to the manufacturing process variation.

In order to maintain a stable system frequency, the values of the Cext should not be less than 20pF, and that the value of Rext should not be greater than 1 MΩ. If they cannot be kept in this range, the frequency can be easily affected by noise, humidity, and leakage.

The smaller the Rext in the RC oscillator is, the faster its frequency will be. On the contrary, for very low Rext values, for instance, 1 KΩ, the oscillator becomes unstable because the NMOS cannot discharge the current of the capacitance correctly.

Based on the above reasons, it must be kept in mind that all of the supply voltage, the operation temperature, the components of the RC oscillator, the package types, the way the PCB is layout, will affect the system frequency.
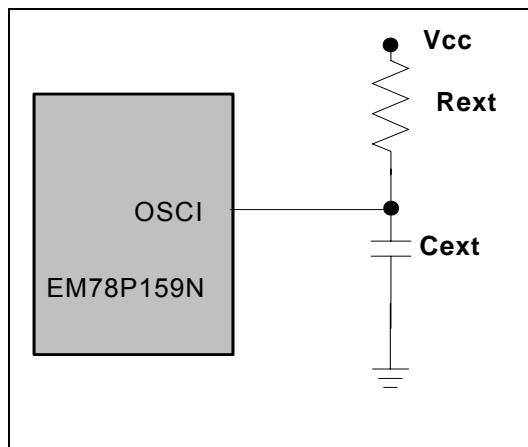
Figure 4-9 External RC Oscillator Mode Circuit

■ **RC Oscillator Frequencies**

Cext	Rext	Average Fosc 5V, 25°C	Average Fosc 3V, 25°C
20 pF	3.3k	3.92 MHz	3.65 MHz
	5.1k	2.67 MHz	2.60 MHz
	10k	1.39MHz	1.40 MHz
	100k	149 kHz	156 kHz
100 pF	3.3k	1.39 MHz	1.33 MHz
	5.1k	940 kHz	920 kHz
	10k	480 kHz	475 kHz
	100k	52 kHz	50 kHz
300 pF	3.3k	595 kHz	560 kHz
	5.1k	400 kHz	390 kHz
	10k	200 kHz	200 kHz
	100k	21 kHz	20 kHz

NOTE

1. *Measured on DIP packages.*

2. *The values are for design reference only.*

3. *The frequency drift is about ±30%*

4.7.4 Internal RC Oscillator Mode

EM78P159N offers a versatile internal RC mode with default frequency value of 4MHz. The Internal RC oscillator mode has other frequencies (1MHz, 8MHz. & 455kHz) that can be set by CODE OPTION (WORD1), RCM1, and RCM0. All these four main frequencies can be calibrated by programming the OPTION Bits C3 ~ C0. The table below describes a typical instance of the calibration.

■ **Internal RC Drift Rate (Ta=25℃, VDD=3.9V±5%, VSS=0V)**

Internal RC Frequency	Drift Rate			
	Temperature (-40℃ ~ +85℃)	Voltage (2.3V ~ 5.5V)	Process	Total
4MHz	±5%	±5%	±4%	±14%
8MHz	±5%	±5%	±4%	±14%
1MHz	±5%	±5%	±4%	±14%
455MHz	±5%	±5%	±4%	±14%

The above are theoretical values and are provided for reference only. Actual values may vary depending on actual process.

■   **Calibration Selection for Internal RC Mode**

C3	C2	C1	C0	Cycle Time (ns)	Frequency (MHz)
0	0	0	0	390.6	2.56
0	0	0	1	365.0	2.74
0	0	1	0	342.5	2.92
0	0	1	1	322.6	3.1
0	1	0	0	304.9	3.28
0	1	0	1	289.0	3.46
0	1	1	0	274.7	3.64
0	1	1	1	261.8	3.82
1	1	1	1	250.0	4.00
1	1	1	0	239.2	4.18
1	1	0	1	229.4	4.36
1	1	0	0	220.3	4.54
1	0	1	1	211.9	4.72
1	0	1	0	204.1	4.9
1	0	0	1	196.7	5.08
1	0	0	0	190.1	5.26

The above are theoretical values and are provided for reference only. Actual values may vary depending on actual process.

4.8 CODE Option Register

The EM78P159N has a CODE option word that is not a part of the normal program memory. The option bits cannot be accessed during normal program execution.

■   **Code Option Register and Customer ID Register Arrangement Distribution:**

Word 0	Word 1	Word 2
Bit12 ~ Bit0	Bit12 ~ Bit0	Bit12 ~ Bit0

4.8.1 Code Option Register (Word 0)

WORD 0												
Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	CLKS0	ENWDTB	OSC2	OSC1	OSC0	HLP	PR2	PR1	PR0

Bit 0 ~ Bit 2 (PR0 ~ PR2): Protect bits

PR0 ~ PR2 are protect bits. Protect types are as follows**:**

PR2	PR1	PR0	Protect
0	0	0	Enable
0	0	1	Enable
0	1	0	Enable
0	1	1	Enable
1	0	0	Enable
1	0	1	Enable
1	1	0	Enable
1	1	1	Disable

Bit 3 (HLP):   Power selection

0 = Low power

1 = High power

Bit 4 ~ Bit 6 (OSC0 ~ OSC2): Oscillator Modes Selection bits

Mode		OSC2	OSC1	OSC0
ERC (External RC oscillator mode); P55/OSCO act P55		0	0	0
ERC (External RC oscillator mode); P55/OSCO act OSCO		0	0	1
IRC (Internal RC oscillator mode) ; P55/OSCO act P55		0	1	0
IRC (Internal RC oscillator mode); P55/OSCO act OSCO		0	1	1
MCIRC (Manual calibration IRC mode); P55/OSCO act P55	With Simulator only	1	0	0
MCIRC (Manual calibration IRC mode); P55/OSCO act OSCO		1	0	1
LXT (Low XTAL oscillator mode)		1	1	0
HXT (High XTAL oscillator mode) **(default)**		1	1	1

NOTE

The transient point of system frequency between HXT and LXY is around 400 KHz.

Bit 7 (ENWDTB): Watchdog timer enable bit.

0 = Enable

1 = Disable

Bit 8 (CLKS0):   Instruction period option bit

Word 0	CLK0
4 oscillator time periods **(default)**	1
2 oscillator time periods	0

Refer to Section 4.12 *Instruction Set* for further details.

Bit 9 ~ Bit 12:   Not used, but need to set to "1" all the time to preclude possible error.

4.8.2 Customer ID Register (Word 1)

WORD 0												
Bit12	**Bit11**	**Bit10**	**Bit9**	**Bit8**	**Bit7**	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**
-	RCOUT	-	-	-	-	CYES	-	-	-	-	RCM1	RCM0

Bit 0 ~ Bit 1 (RCM0 ~ RCM1): IRC mode selection bits

RCM 1	RCM 0	Frequency (MHz)
1	1	4
1	0	8
0	1	1
0	0	455kHz

Bit 2 ~ Bit 5:   Not used

Bit 6 (CYES): Instruction cycle selection bit
0 = one instruction cycle
1 = two instruction cycles (default)

Bit 7 ~ Bit 10: Not used

Bits 11 (RCOUT): System clock output enable bit in IRC or ERC mode
0 = OSCO pin is open drain.
1 = OSCO output system clock

Bit 12: Not used

4.8.3 Customer ID Register (Word 2)

WORD 0												
Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
-	-	-	-	-	-	-	-	-	-	-	-	-

Bit 0 ~ Bit 12: User's ID code

4.9 Power On Considerations

Any microcontroller is not guaranteed to start to operate properly before the power supply stays at its steady state.

EM78P159N POR voltage range is 1.7V~1.9V. Under customer application, when power is OFF, Vdd must drop to below 1.2V and remains OFF for 10μs before power can be switched ON again. This way, the EM78P159N will reset and operates normally. The extra external reset circuit will work well if Vdd can rise at very fast speed (50 ms or less). However, under most cases where critical applications are involved, extra devices are required to assist in solving the power-up problems.

4.10 External Power On Reset Circuit

The circuit shown in the following figure implements an external RC to produce the reset pulse. The pulse width (time constant) should be kept long enough for Vdd to reached minimum operation voltage. This circuit is used when the power supply has a slow rise time. Because the current

Figure 4-10 External Power-Up Reset Circuit

leakage from the /RESET pin is about ±5μA, it is recommended that R should not be greater than 40K. In this way, the /RESET pin voltage is held below 0.2V. The diode (D) acts as a short circuit at the moment of power down. The capacitor C will discharge rapidly and fully. Rin, the current-limited resistor, will prevent high current or ESD (electrostatic discharge) from flowing to pin /RESET.

4.11 Residue-Voltage Protection

When the battery is replaced, device power (Vdd) is cut off but residue-voltage remains. The residue-voltage may trips below minimum Vdd, but not to zero. This condition may cause a poor power-on reset. The following figures illustrate two recommended methods on how to build a residue-voltage protection circuit for EM78P159N.
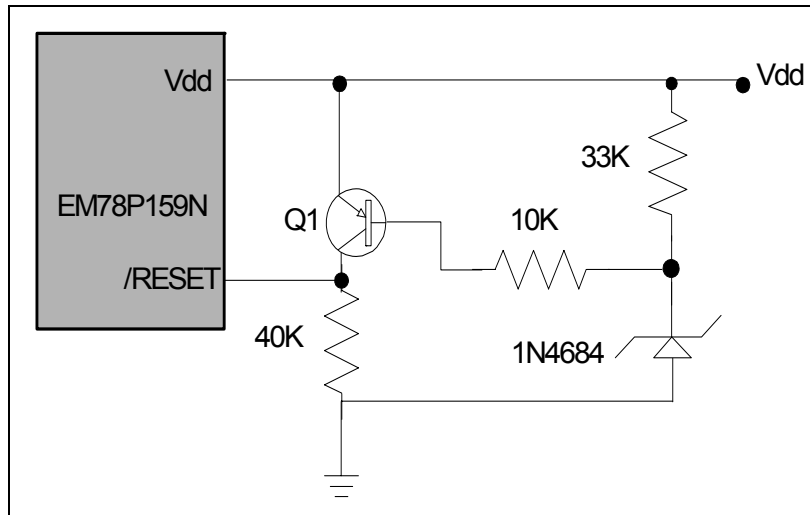
Figure 4-11a Residue Voltage Protection Circuit (1)
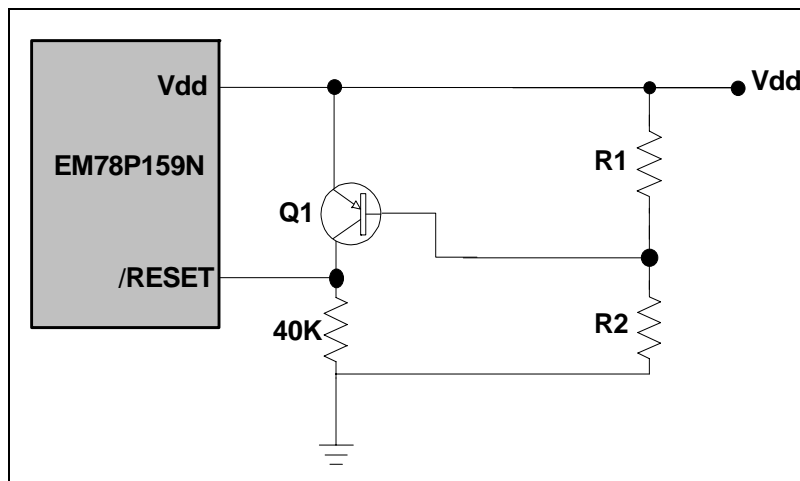
Figure 4-11b Residue Voltage Protection Circuit (2)

4.12 Instruction Set

Each instruction in the instruction set is a 13-bit word divided into an OP code and one or more operands. Normally, all instructions are executed within one single instruction cycle (one instruction consists of 2 oscillator periods), unless the program counter is changed by instruction "MOV R2,A", "ADD R2,A", or by instructions of arithmetic or logic operation on R2 (e.g., "SUB R2,A", "BS(C) R2,6", "CLR R2", ····). In this case, the execution takes two instruction cycles.

If for some reasons, the specification of the instruction cycle is not suitable for certain applications, try modifying the instruction as follows**:**

(A) Change one instruction cycle to consist of 4 oscillator periods.

(B) "JMP," "CALL," "RET," "RETL," "RETI," or the conditional skip ("JBS," "JBC," "JZ," "JZA," "DJZ," "DJZA") commands which were tested to be true, are executed within two instruction cycles. The instructions that are written to the program counter also take two instruction cycles.

Case (A) is selected by the CODE Option bit, called CLK. One instruction cycle consists of two oscillator clocks if CLK is low, and four oscillator clocks if CLK is high.

Note that once the 4 oscillator periods within one instruction cycle is selected as in Case (A), the internal clock source to TCC should be CLK=Fosc/4, instead of Fosc/ 2.

Moreover, the instruction set has the following features**:**

1) Every bit of any register can be set, cleared, or tested directly.

2) The I/O register can be regarded as general register. That is, the same instruction can operate on I/O register.

The following symbols are used in the following Instruction Set table**:**

R represents a register designator that specifies which one of the registers (including operational registers and general purpose registers) is to be utilized by the instruction.

b represents a bit field designator that selects the value for the bit which is located in the register "R", and affects operation.

K represents an 8 or 10-bit constant or literal value.

Instruction Binary	Hex	Mnemonic	Operation	Status Affected
0 0000 0000 0000	0000	NOP	No Operation	None
0 0000 0000 0001	0001	DAA	Decimal Adjust A	C
0 0000 0000 0010	0002	CONTW	A → CONT	None
0 0000 0000 0011	0003	SLEP	0 → WDT, Stop oscillator	T,P
0 0000 0000 0100	0004	WDTC	0 → WDT	T,P
0 0000 0000 rrrr	000r	IOW R	A → IOCR	None <**Note1**>
0 0000 0001 0000	0010	ENI	Enable Interrupt	None
0 0000 0001 0001	0011	DISI	Disable Interrupt	None
0 0000 0001 0010	0012	RET	[Top of Stack] → PC	None
0 0000 0001 0011	0013	RETI	[Top of Stack] → PC, Enable Interrupt	None
0 0000 0001 0100	0014	CONTR	CONT → A	None
0 0000 0001 rrrr	001r	IOR R	IOCR → A	None <**Note1**>
0 0000 01rr rrrr	00rr	MOV R,A	A → R	None
0 0000 1000 0000	0080	CLRA	0 → A	Z
0 0000 11rr rrrr	00rr	CLR R	0 → R	Z
0 0001 00rr rrrr	01rr	SUB A,R	R-A → A	Z,C,DC
0 0001 01rr rrrr	01rr	SUB R,A	R-A → R	Z,C,DC
0 0001 10rr rrrr	01rr	DECA R	R-1 → A	Z
0 0001 11rr rrrr	01rr	DEC R	R-1 → R	Z
0 0010 00rr rrrr	02rr	OR A,R	A ∨ R → A	Z
0 0010 01rr rrrr	02rr	OR R,A	A ∨ R → R	Z
0 0010 10rr rrrr	02rr	AND A,R	A & R → A	Z
0 0010 11rr rrrr	02rr	AND R,A	A & R → R	Z
0 0011 00rr rrrr	03rr	XOR A,R	A ⊕ R → A	Z
0 0011 01rr rrrr	03rr	XOR R,A	A ⊕ R → R	Z
0 0011 10rr rrrr	03rr	ADD A,R	A + R → A	Z,C,DC
0 0011 11rr rrrr	03rr	ADD R,A	A + R → R	Z,C,DC
0 0100 00rr rrrr	04rr	MOV A,R	R → A	Z
0 0100 01rr rrrr	04rr	MOV R,R	R → R	Z
0 0100 10rr rrrr	04rr	COMA R	/R → A	Z
0 0100 11rr rrrr	04rr	COM R	/R → R	Z
0 0101 00rr rrrr	05rr	INCA R	R+1 → A	Z
0 0101 01rr rrrr	05rr	INC R	R+1 → R	Z
0 0101 10rr rrrr	05rr	DJZA R	R-1 → A, skip if zero	None
0 0101 11rr rrrr	05rr	DJZ R	R-1 → R, skip if zero	None
0 0110 00rr rrrr	06rr	RRCA R	R(n) → A(n-1), R(0) → C, C → A(7)	C
0 0110 01rr rrrr	06rr	RRC R	R(n) → R(n-1), R(0) → C, C → R(7)	C

Instruction Binary	Hex	Mnemonic	Operation	Status Affected
0 0110 10rr rrrr	06rr	RLCA R	R(n) → A(n+1), R(7) → C, C → A(0)	C
0 0110 11rr rrrr	06rr	RLC R	R(n) → R(n+1), R(7) → C, C → R(0)	C
0 0111 00rr rrrr	07rr	SWAPA R	R(0-3) → A(4-7), R(4-7) → A(0-3)	None
0 0111 01rr rrrr	07rr	SWAP R	R(0-3) ↔ R(4-7)	None
0 0111 10rr rrrr	07rr	JZA R	R+1 → A, skip if zero	None
0 0111 11rr rrrr	07rr	JZ R	R+1 → R, skip if zero	None
0 100b bbrr rrrr	0xxx	BC R,b	0 → R(b)	None <**Note2**>
0 101b bbrr rrrr	0xxx	BS R,b	1 → R(b)	None <**Note3**>
0 110b bbrr rrrr	0xxx	JBC R,b	if R(b)=0, skip	None
0 111b bbrr rrrr	0xxx	JBS R,b	if R(b)=1, skip	None
1 00kk kkkk kkkk	1kkk	CALL k	PC+1 → [SP], (Page, k) → PC	None
1 01kk kkkk kkkk	1kkk	JMP k	(Page, k) → PC	None
1 1000 kkkk kkkk	18kk	MOV A,k	k → A	None
1 1001 kkkk kkkk	19kk	OR A,k	A ∨ k → A	Z
1 1010 kkkk kkkk	1Akk	AND A,k	A & k → A	Z
1 1011 kkkk kkkk	1Bkk	XOR A,k	A ⊕ k → A	Z
1 1100 kkkk kkkk	1Ckk	RETL k	k → A, [Top of Stack] → PC	None
1 1101 kkkk kkkk	1Dkk	SUB A,k	k-A → A	Z,C,DC
1 1110 0000 0001	1E01	INT	PC+1 → [SP], 001H → PC	None
1 1111 kkkk kkkk	1Fkk	ADD A,k	k+A → A	Z,C,DC

Note 1: This instruction is applicable to IOC5~IOC6, IOCB~IOCF only.

Note 2: This instruction is not recommended for RF operation.

Note 3: This instruction cannot operate under RF.

4.13 Timing Diagrams

AC Test Input/Output Waveform

VDD-0.5V

0.75VDD   0.75VDD
                TEST POINTS
0.25VDD   0.25VDD

GND+0.5V

AC Testing : Input is driven at VDD-0.5V for logic "1",and GND+0.5V for logic "0".Timing measurements are made at 0.75VDD for logic "1",and 0.25VDD for logic "0".

RESET Timing (CLK="0")

NOP

Instruction 1
Executed

CLK

/RESET

Tdrh

TCC Input Timing (CLKS="0")

Tins

CLK

TCC

Ttcc
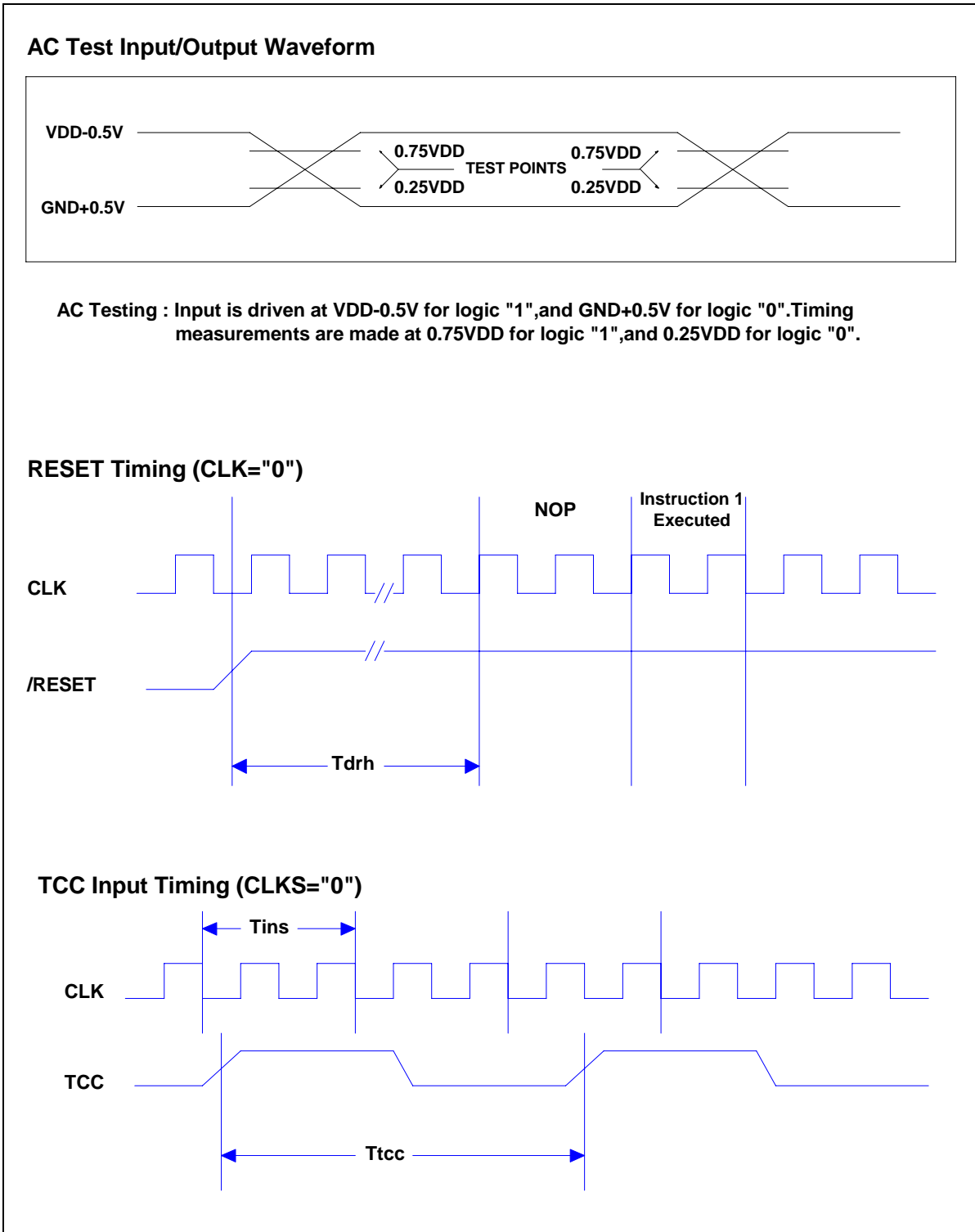
Figure 4-12   EM78P159N Timing Diagrams

5   Absolute Maximunm Ratings

■   **EM78P159N**

Items	Rating
Temperature under bias	-40°C to 85°C
Storage temperature	-65°C to 150°C
Working voltage	2.1 to 5.5V
Working frequency	DC to 20MHz*
Input voltage	Vss-0.3V to Vdd+0.5V
Output voltage	Vss-0.3V to Vdd+0.5V

These parameters are theoretical values and have not been tested.

6   Electrical Characteristics

6.1 DC Electrical Characteristic

■   **(Ta=25 °C, VDD=5V±5%, VSS=0V)**

Symbol	Parameter	Condition	Min	Typ	Max	Unit
FXT	XTAL: VDD to 3V	Two cycle with two clocks	DC		8.0	MHz
	XTAL: VDD to 5V	Two cycle with two clocks	DC		20.0	MHz
ERC	ERC: VDD to 5V	R: 5.1KΩ, C: 100 pF	F±30%	940	F±30%	KHz
IIL	Input Leakage Current for input pins	VIN = VDD, VSS			±1	μA
VIH1	Input High Voltage (VDD=5V)	Ports 5, 6 (Schmitt trigger)	0.75Vdd		Vdd+0.3	V
VIL1	Input Low Voltage (VDD=5V)	Ports 5, 6 (Schmitt trigger)	Vdd-0.3		0.25Vdd	V
VIHT1	Input High Threshold Voltage (VDD=5V)	/RESET, TCC (Schmitt trigger)	0.75Vdd		Vdd+0.3	V
VILT1	Input Low Threshold Voltage (VDD=5V)	/RESET, TCC (Schmitt trigger)	Vdd-0.3		0.25Vdd	V
VIHX1	Clock Input High Voltage (VDD=5V)	OSCI (Schmitt trigger)	0.75Vdd		Vdd+0.3	V
VILX1	Clock Input Low Voltage (VDD=5V)	OSCI (Schmitt trigger)	Vdd-0.3		0.25Vdd	V
VIH2	Input High Voltage (VDD=3V)	Ports 5, 6 (Schmitt trigger)	0.75Vdd		Vdd+0.3	V
VIL2	Input Low Voltage (VDD=3V)	Ports 5, 6 (Schmitt trigger)	Vdd-0.3		0.25Vdd	V
VIHT2	Input High Threshold Voltage (VDD=3V)	/RESET, TCC (Schmitt trigger)	0.75Vdd		Vdd+0.3	V
VILT2	Input Low Threshold Voltage (VDD=3V)	/RESET, TCC (Schmitt trigger)	Vdd-0.3		0.25Vdd	V
VIHX2	Clock Input High Voltage (VDD=3V)	OSCI (Schmitt trigger)	0.75Vdd		Vdd+0.3	V
VILX2	Clock Input Low Voltage (VDD=3V)	OSCI (Schmitt trigger)	Vdd-0.3		0.25Vdd	V
VOH1	Output High Voltage (Ports 5)	IOH = -6 mA	4.5			V
VOH1	Output High Voltage (Ports 6) (Schmitt trigger)	IOH = -6 mA	4.5			V
VOL1	Output Low Voltage(Port5)	IOL = 16.5 mA			0.5	V
VOL1	Output Low Voltage (Ports 6) (Schmitt trigger)	IOL = 16.5 mA			0.5	V
IPH	Pull-high current	Pull-high active, input pin at VSS	–50	–70	–100	μA
IPD	Pull-down current	Pull-down active, input pin at VDD	25	50	120	μA

Symbol	Parameter	Condition	Min	Typ	Max	Unit
ISB1	Power down current (VDD=5.0V)	All input and I/O pins at VDD, output pin floating, WDT disabled		1	2	µA
ISB2	Power down current (VDD=5.0V)	All input and I/O pins at VDD, output pin floating, WDT enabled		6	10	µA
ICC1	Operating supply current (VDD=3V) at two cycles/four clocks	/RESET= 'High', Fosc=32KHz (Crystal type,CLKS="0"), output pin floating, WDT disabled		20	30	µA
ICC2	Operating supply current (VDD=3V) at two cycles/four clocks	/RESET= 'High', Fosc=32KHz (Crystal type,CLKS="0"), output pin floating, WDT enabled		22	32	µA
ICC3	Operating supply current (VDD=5.0V) at two cycles/two clocks	/RESET= 'High', Fosc=4MHz (Crystal type, CLKS="0"), output pin floating, WDT enabled		1.7	2.5	mA
ICC4	Operating supply current (VDD=5.0V) at two cycles/four clocks	/RESET= 'High', Fosc=10MHz (Crystal type, CLKS="0"), output pin floating, WDT enabled		2.7	3.5	mA

These parameters are theoretical values and have not been tested.

6.2 AC Electrical Characteristic

■ **(Ta=25 °C, VDD=5V±5%, VSS=0V)**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Dclk	Input CLK duty cycle		45	50	55	%
Tins	Instruction cycle time (CLKS="0")	Crystal type	100		DC	ns
		RC type	500		DC	ns
Ttcc	TCC input period		(Tins+20)/N*			ns
Tdrh	Device reset hold time		11.8	16.8	21.8	ms
Trst	/RESET pulse width	Ta = 25°C	2000			ns
Twdt	Watchdog timer period	Ta = 25°C	11.8	16.8	21.8	ms
Tset	Input pin setup time			0		ns
Thold	Input pin hold time			20		ns
Tdelay	Output pin delay time	Cload=20pF		50		ns

* N = selected prescaler ratio.

These parameters are theoretical values and have not been tested.

Data in the Minimum, Typical, Maximum ("Min","Typ","Max") columns are based on characterization results at 25℃. This data is for design reference only and has not been tested.

APPENDIX

A Package Types

OTP MCU	Package Type	Pin Count	Package Size
EM78P159NP	DIP	18	300 mil
EM78P159NM	SOP	18	300 mil
EM78159NAS	SSOP	20	209 mil
EM78159NKM	SSOP	20	209 mil

B Package Information

■ **18-Lead Plastic Dual in Line (PDIP) — 300 mil**

Symbol	Min	Normal	Max
A			4.450
A1	0.381		
A2	3.175	3.302	3.429
c	0.203	0.254	0.356
D	22.610	22.860	23.110
E1	6.220	6.438	6.655
E	7.370	7.620	7.870
eB	8.510	9.020	9.530
B	0.356	0.457	0.559
B1	1.143	1.524	1.778
L	3.048	3.302	3.556
e	2.540(TYP)		
θ	0		15

TITLE:
PDIP-18L 300MIL PACKAGE OUTLINE DIMENSION

File : D18

Edition: A

Unit : mm
Scale: Free
Material:
Sheet:1 of 1
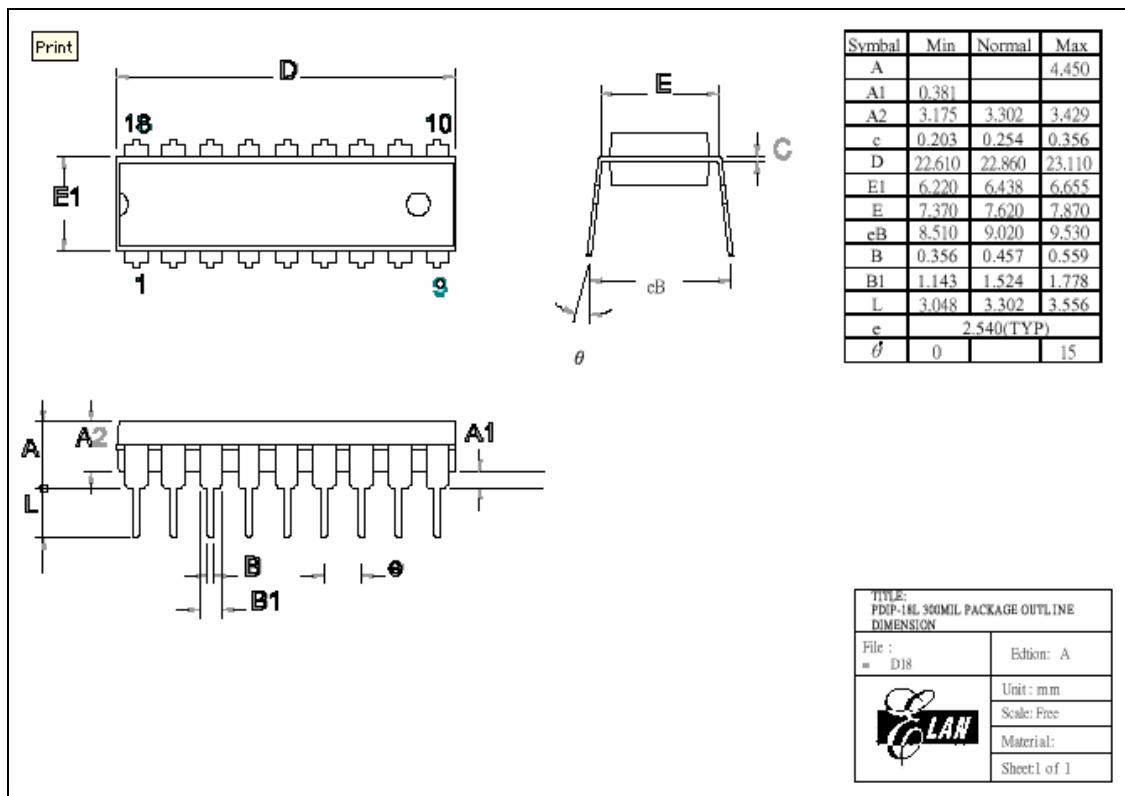
Figure B-1a EM78P159N 18-Lead PDIP Package Type

■ **18-Lead Plastic Small Outline (SOP)** — **300 mil**

Symbol	Min	Normal	Max
A	2.350		2.650
A1	0.102		0.300
b		0.406(TYP)	
c	0.230		0.320
E	7.400		7.600
H	10.000		10.650
D	11.350		11.750
L	0.406	0.838	1.270
e		1.27(TYP)	
θ°	0		8

TITLE:
SOP-18L(300MIL) PACKAGE OUTLINE DIMENSION

File: SO18 — Edtion: A

Unit: mm
Scale: Free
Material:
Sheet:1 of 1
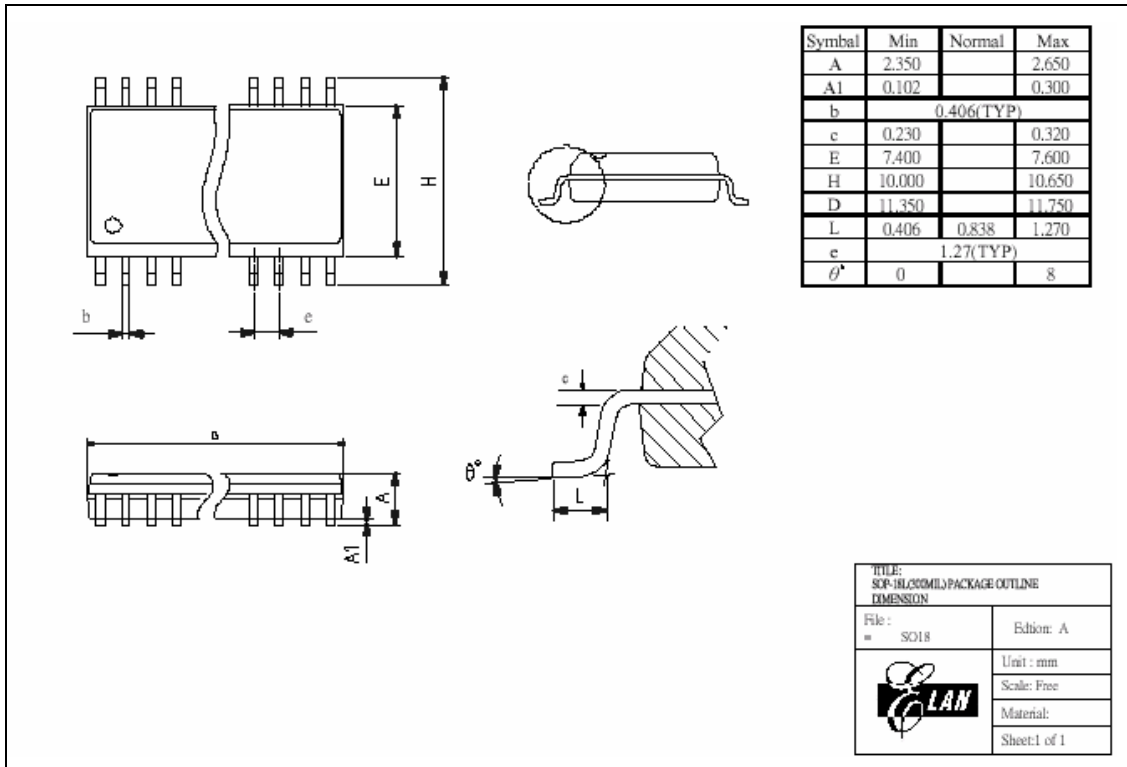
Figure B-1b EM78P159N 18-Lead SOP Package Type

■ **20-Lead Plastic Small Outline (SSOP)** — **209 mil**

Symbol	Min	Normal	Max
A			2.130
A1	0.050		0.250
A2	1.620	1.750	1.880
b	0.220		0.380
c	0.090		0.200
E	7.400	7.800	8.200
E1	5.000	5.300	5.600
D	6.900	7.200	7.500
L	0.650	0.750	0.850
L1		1.250(REF)	
e		0.650(TYP)	
θ°	0	4	8

File: SSOP20 — Edtion: A

Unit: mm
Scale: Free
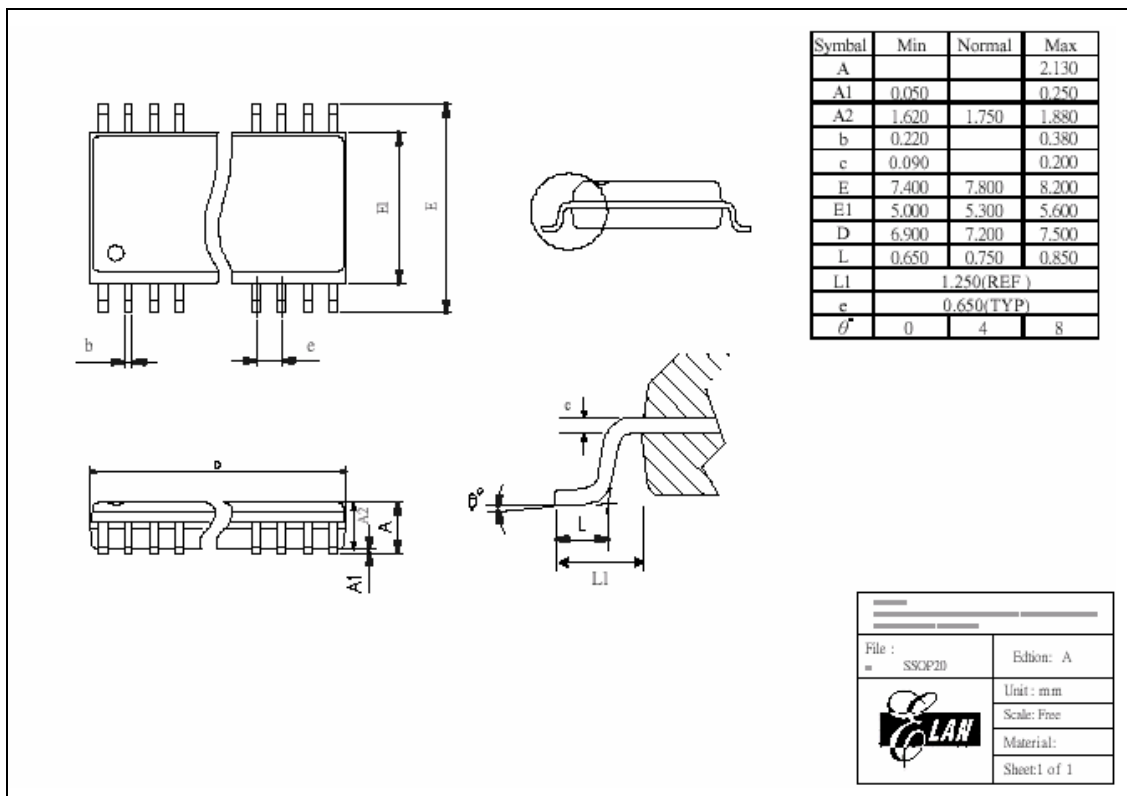Material:
Sheet:1 of 1

Figure B-1c EM78P159N 20-Lead SSOP Package Type

C   Quality Assurance and Reliability

C.1 Reliability Test

Test Category	Test Conditions	Remarks
Solderability	Solder temperature = 245±5°C for 5 seconds up to the stopper using a rosin-type flux	
Pre-condition	Step 1**:** TCT 65°C (15mins) ~ 150°C (15mins), 10 cycles	For SMD IC (such as SOP, QFP, SOJ, etc.)
	Step 2**:** bake 125°C, TD(endurance) = 24 hrs.	
	Step 3**:** soak 30°C /60%, TD (endurance) = 192hrs.	
	Step 4**:** IR flow 3cycles (Pkg thickness ≥ 2.5mm or Pkg volume ≥ 350mm3--225±5°C) (Pkg thickness ≤ 2.5mm or Pkg volume ≤ 350mm3--240±5°C)	
Temperature cycle test	–65°C (15mins) ~ 150°C (15mins), 200 cycles	
Pressure cooker test	TA =121°C, RH = 100%, pressure = 2atm, TD (endurance) = 96 Hrs.	
High temperature /high humidity test	TA=85°C , RH=85%, TD (endurance) = 168, 500 Hrs	
High-temperature storage life	TA=150°C, TD (endurance) = 500, 1000Hrs.	
High-temperature operating life	TA=125°C, VCC = Max. operating voltage, TD (endurance) = 168,500, 1000Hrs.	
Latch-up	TA=25°C, VCC = Max. operating voltage, 150mA/20V	
ESD (HBM)	TA=25°C, ≥ ±3KV	IP_ND,OP_ND,IO_ND IP_NS,OP_NS,IO_NS IP_PD,OP_PD,IO_PD, IP_PS,OP_PS,IO_PS, VDD-VSS(+), VDD_VSS(-)mode
ESD (MM)	TA=25°C, ≥ ±300V	

C.2 Power-On Reset and Vdd Voltage Drop/Rise Timing Test
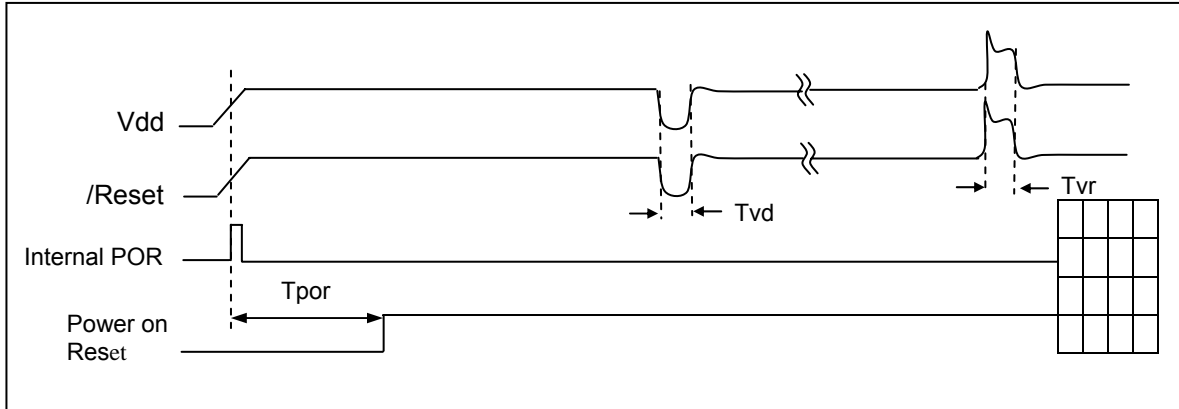
Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Tpor	Power on reset time	Vdd = 5V, -40℃ to 85℃	10.5	16.8	22	ms
Tvd*	Vdd Voltage drop time	Vdd = 5V, -40℃ to 85℃	-	-	1	μs
Tvr**	Vdd Voltage rise time	Vdd = 5V, -40℃ to 85℃	-	-	1	us

* Tvd is the period of Vdd voltage lower than POR voltage.

** Tvr is the period of Vdd voltage higher than 5.5V.

Figure C-1 EM78P159N Power-On Reset and Vdd Voltage Drop/Rise Timing Test Timing Diagram

C.3 Address Trap Detect

An address trap detect is one of the fail-safe function that detects CPU malfunction caused by noise or the like. If the CPU attempts to fetch an instruction from a part of RAM, an internal recovery circuit will be auto started. Until CPU got the correct function, it will execute the next program.