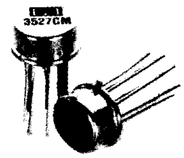
BURR-BROWN

3527



Low Drift - Low Bias Current FET Input OPERATIONAL AMPLIFIER

FEATURES

- LOWER PRICED
- ULTRA-LOW DRIFT, 2μV/°C, max
- LOW INITIAL OFFSET VOLTAGE, 250μV, max
- LOW BIAS CURRENT, 2pA, max
- LOW NOISE

APPLICATIONS

- CURRENT-TO-VOLTAGE CONVERSION
- LONG TERM INTEGRATION
- LOW DROOP SAMPLE/HOLD CIRCUITS
- PRECISION VOLTAGE AMPLIFICATION
- HIGH INPUT RESISTANCE BUFFER

DESCRIPTION

The Burr-Brown 3527 is a precision operational amplifier. It offers excellent performance at moderate cost through the use of hybrid construction, monolithic ICs, matched FETs, thin-film resistors, and active laser trimming.

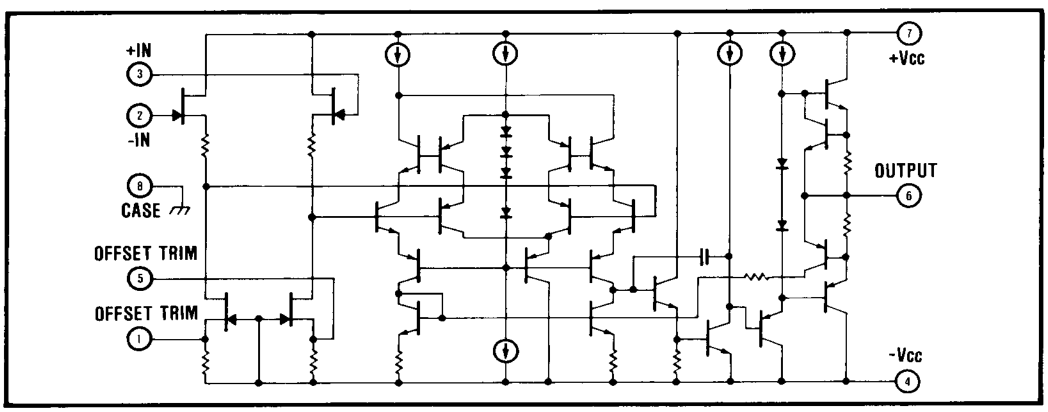
The 3527 low, initial offset voltage (250μV max) allows higher design accuracy at lower installed cost. Costly pots and external nulling of the offset voltage are not required for most applications. Also, higher system reliability is achieved by using fewer parts.

The offset voltage temperature drift of the 3527 is exceptionally low (2μV/°C max) and is compatible with the best bipolar amplifiers (BB3500E). It is achieved by laser adjusting the offset during manufacture and means that high system accuracy is maintained over the temperature range.

The low bias current (guaranteed 2pA max) allows the use of larger feedback resistor values, and smaller bias current errors are realizable.

Of course, all the other desirable features of high quality op amps are engineered into the 3527. It has low input noise, is free from latch up, is short circuit protected for continuous output shorts to common, is internally compensated for unity gain stability, and is pin compatible with 741 amplifiers. Guarding is achieved by the pin 8 case connection.

For increased reliability screening, consult Burr-Brown.



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PDS-370B

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SPECIFICATIONS

ELECTRICAL

Specifications typical at T_A = 25°C and ±15VDC supplies, unless otherwise noted.

MODELS	3527AM Min	3527AM Typ	3527AM Max	3527BM Min	3527BM Typ	3527BM Max	3527CM Min	3527CM Typ	3527CM Max	Units
OPEN LOOP GAIN, DC										
No Load		112			*			*		dB
R_L = 2kΩ	100	108		*	*		*	*		dB
RATED OUTPUT										
Voltage	±10	±12		*	*		*	*		V
Current	±10	±20		*	*		*	*		mA
Output Impedance		600			*			*		Ω
Load Capacitance		1000			*			*		pF
FREQUENCY RESPONSE										
Unity Gain, Open Loop		1			*			*		MHz
Full Power Response	10	14		*	*		*	*		kHz
Slew Rate	0.6	0.9		*	*		*	*		V/μsec
Settling Time (0.01%)		45			*			*		μsec
INPUT OFFSET VOLTAGE										
Initial Offset, 25°C		±200	±500		±100	±250		±100	±250	μV
vs. Temp. (-25°C to +85°C)		±5	±10		±2	±5		±1	±2	μV/°C
vs. Supply Voltage		±75			*			*		μV/V
vs. Time		±20			*			*		μV/mo
INPUT BIAS CURRENT										
Initial Bias, 25°C		-2	-5		-0.7	-2		-2	-5	pA
vs. Temp		**			**			**		
vs. Supply Voltage		±5			*			*		pA/V
INPUT DIFFERENCE CURRENT										
Initial Difference, 25°C		±0.3			*			*		pA
INPUT IMPEDANCE										
Differential		10^{12}			*			*		Ω
Common-mode		10^{15}			*			*		Ω
INPUT NOISE										
Voltage, f_o = 10Hz		75			*			*		nV/√Hz
f_o = 100Hz		35			*			*		nV/√Hz
f_o = 1kHz		30			*			*		nV/√Hz
f_o = 10kHz		25			*			*		nV/√Hz
0.3Hz to 10Hz, p-p		2.6			*			*		μV
10Hz to 10kHz, rms		3			*			*		μV
Current, 0.3Hz to 10Hz, p-p		15			*			*		fA
10Hz to 10kHz, rms		60			*			*		fA
INPUT VOLTAGE RANGE										
Common-mode Voltage Range		±(|Vs|-3)			*			*		V
Common-mode Rejection at ±10V		76			*			*		dB
Max. Safe Input Voltage		±Vs			*			*		VDC
POWER SUPPLY										
Rated Voltage		±15			*			*		VDC
Voltage Range, derated performance	±5		±20	*		*	*		*	VDC
Current, quiescent		2.6	4		*	*		*	*	mA
TEMPERATURE RANGE (ambient)										
Specification	-25		+85	*		*	*		*	°C
Operating	-55		+125	*		*	*		*	°C
Storage	-65		+150	*		*	*		*	°C
θ junction-ambient		235			*			*		°C/W

*Specifications same as for 3527AM.
**Doubles every +10°C.

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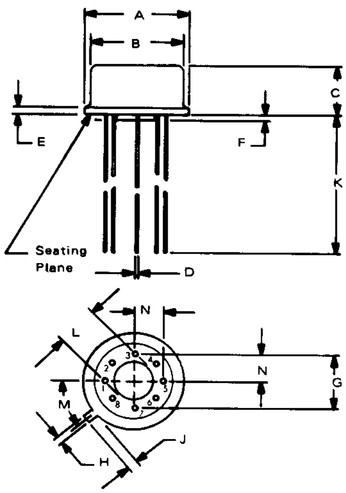
MECHANICAL TO-99 PACKAGE

Order Number: 3527AM, 3527BM, 3527CM Weight: 1 gram



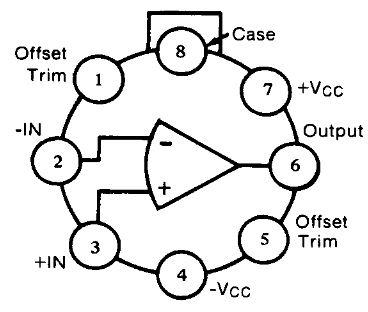
NOTE:
Leads in true position within .010" (.25mm) R at MMC at seating plane.

Pin numbers shown for reference only. Numbers may not be marked on package.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.335	.370	8.51	9.40
B	.305	.335	7.75	8.51
C	.165	.185	4.19	4.70
D	.016	.021	0.41	0.53
E	.010	.040	0.25	1.02
F	.010	.040	0.25	1.02
G	.200 BASIC		5.08 BASIC	
H	.028	.034	0.71	0.86
J	.029	.045	0.74	1.14
K	.500	--	12.7	--
L	.110	.160	2.79	4.06
M	45° BASIC		45° BASIC	
N	.095	.105	2.41	2.67

Pin material and plating composition conform to method 2003 (solderability) of MIL-STD-883 (except paragraph 3.2)

CONNECTION DIAGRAM

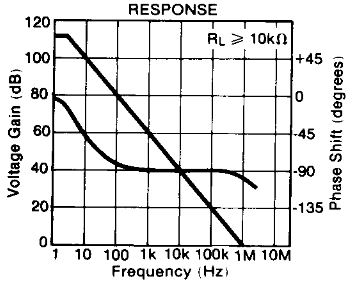


(TOP VIEW)

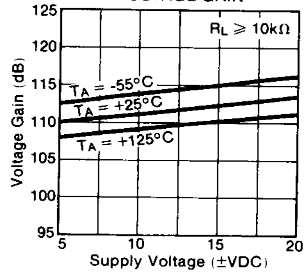
TYPICAL PERFORMANCE CURVES

At $T_A = +25°C$ and ±15VDC supplies, unless otherwise noted.

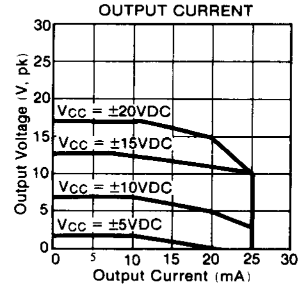
OPEN-LOOP FREQUENCY RESPONSE



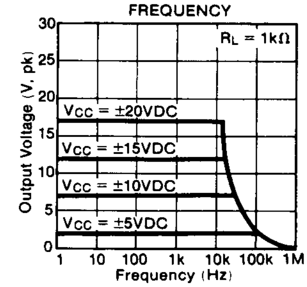
VOLTAGE GAIN



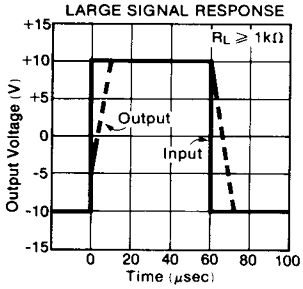
OUTPUT VOLTAGE vs OUTPUT CURRENT



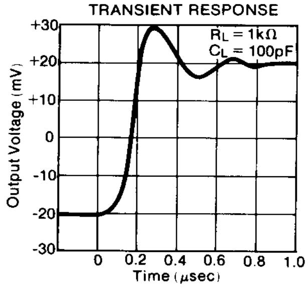
OUTPUT VOLTAGE vs FREQUENCY



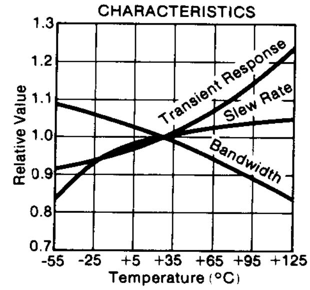
VOLTAGE FOLLOWER LARGE SIGNAL RESPONSE



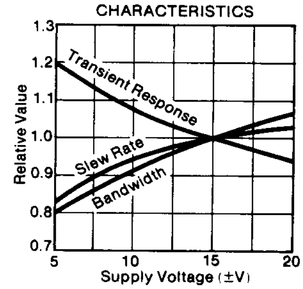
TRANSIENT RESPONSE



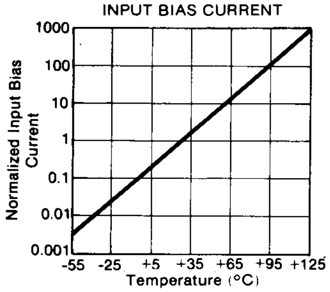
FREQUENCY CHARACTERISTICS



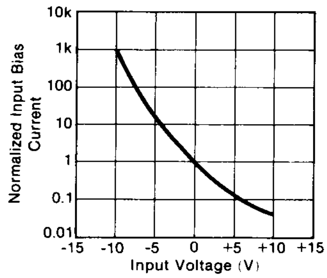
FREQUENCY CHARACTERISTICS



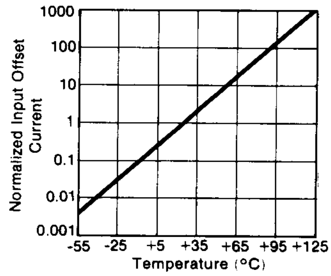
INPUT BIAS CURRENT



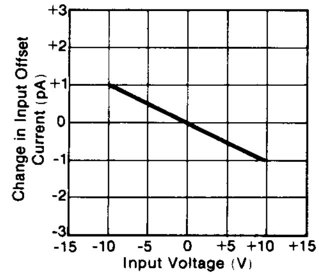
INPUT BIAS CURRENT



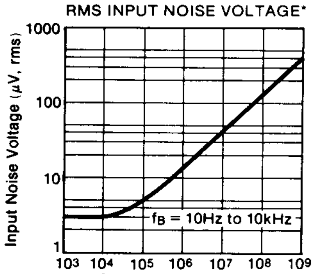
INPUT OFFSET CURRENT



INPUT OFFSET CURRENT

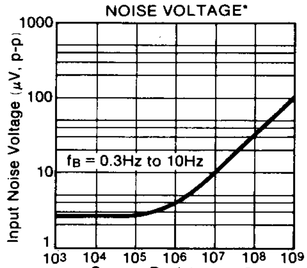


RMS INPUT NOISE VOLTAGE*

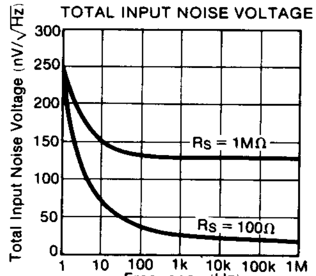


*Includes contribution from source resistance.

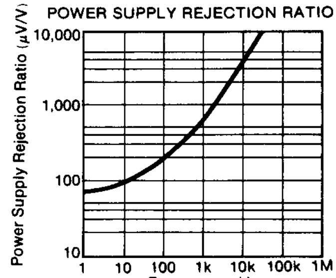
PEAK-TO-PEAK INPUT NOISE VOLTAGE*



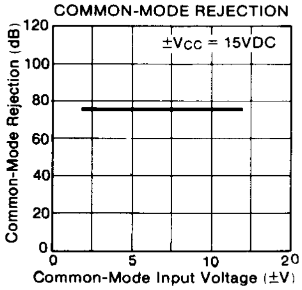
TOTAL INPUT NOISE VOLTAGE



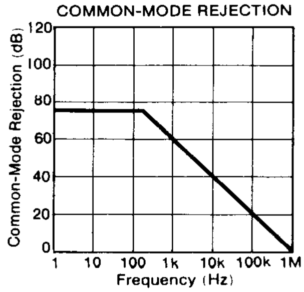
POWER SUPPLY REJECTION RATIO



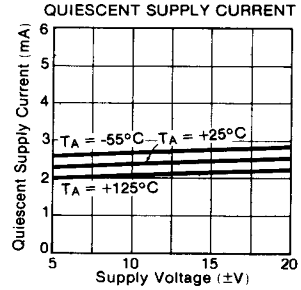
COMMON-MODE REJECTION



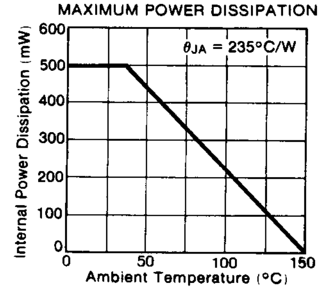
COMMON-MODE REJECTION



QUIESCENT SUPPLY CURRENT



MAXIMUM POWER DISSIPATION



APPLICATIONS INFORMATION

THERMAL RESPONSE TIME

Thermal response time is an important parameter in low drift operational amplifiers like the 3527. A low drift specification would be of little value if the amplifier took several hours to stabilize after turn-on or ambient temperature change. The TO-99 packaging is particularly well suited for devices requiring fast thermal response. Figure 1 shows the typical warm-up drift of the 3527. Note that the offset voltage has stabilized in less than 1 minute. Similar warm-up times for some low drift operational amplifiers ranges from 2 to 15 minutes.

Offset voltage response to thermal shock can provide some real surprises, particularly for amplifiers packaged in discrete modules. Again the 3527 TO-99 package proves superior. Figure 2 shows that the response to thermal shock settles very quickly. The 3527 quickly and smoothly assumes a new value of offset voltage as dictated by the drift specification.

GUARDING AND SHIELDING

The ultra-low bias current and high input impedance of the 3527 are well-suited to a number of stringent applications. However, careless signal wiring of printed circuit board layout can degrade circuit performance several orders of magnitude below the capability of the 3527.

As in any situation where high impedances are involved, careful shielding is required to reduce "hum" pickup in input leads. If large feedback resistors are used, they should also be shielded along with the external input circuitry.

Leakage currents across printed circuit boards can easily exceed the bias current of the 3527. To avoid leakage problems, it is recommended that the signal input lead of the 3527 be wired to a Teflon standoff. If the 3527 is to be soldered directly into a printed circuit board, utmost care must be used in planning the board layout. A "guard" pattern should completely surround the two amplifier input leads and should be connected to a low impedance point which is at the signal input potential.

The amplifier case should be connected to any input shield or guard via pin 8. This insures that the amplifier itself is fully surrounded by guard potential, minimizing both leakage and noise pickup. Figure 3 illustrates the use of the guard.

OFFSET VOLTAGE ADJUSTMENT

Although the 3527 has a low initial offset voltage (250μV), some applications may require external nulling of this small offset. Figure 4 shows the recommended circuit for adjustment of the offset voltage. External offset voltage adjustment changes the laser adjusted offset voltage temperature drift slightly. For each microvolt of offset adjusted, an additional drift of $\pm 0.002\mu V/°C$ is induced.

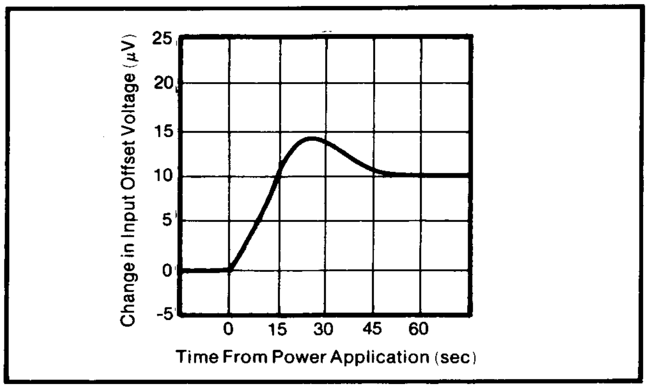


FIGURE 1. Typical Warmup Drift.

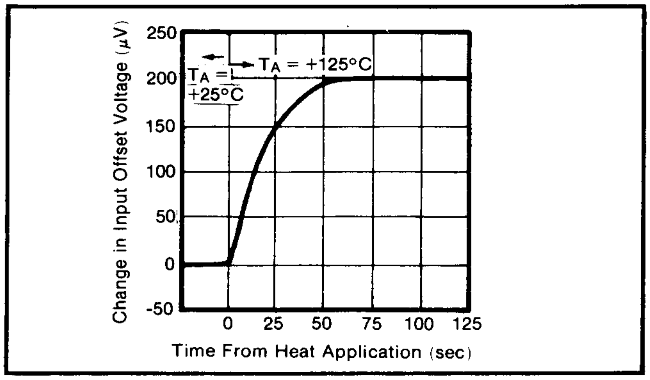


FIGURE 2. Effect of Thermal Shock on Offset Voltage.

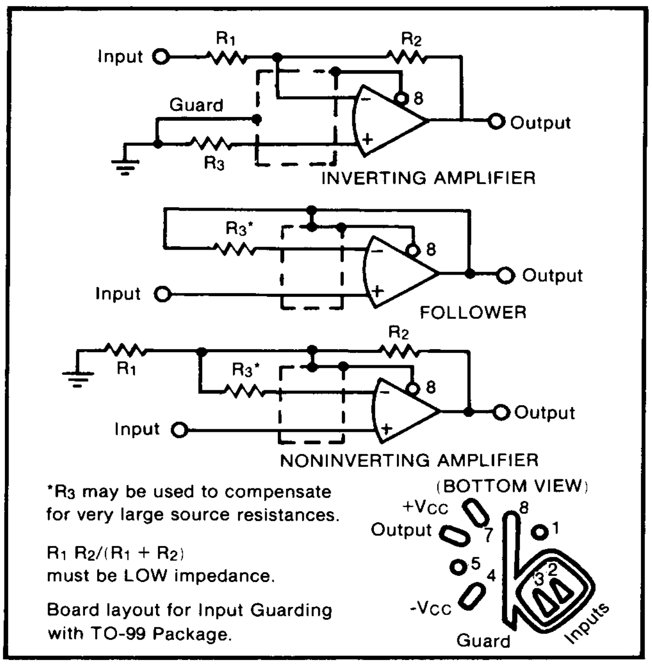


FIGURE 3. Connection of Input Guard.

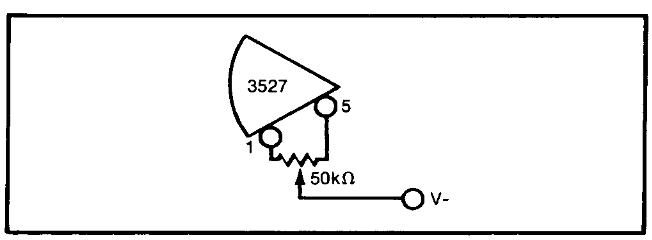


FIGURE 4. External Nulling of Offset Voltage.

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